PRODUCT DESCRIPTION

DXX PLUG-IN UNIT, 2 CARD FOR RBS 2000

RBS2000 two slot Transport Module

DOCUMENT INFORMATION

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1. OVERVIEW

The DXX plug-in unit, 2 Card for RBS 2000 is a double slot Transport Module (TM), that fits into the Six TRX RBS 2000 macro radio cabinets (RBS 2102 and RBS 2202). It has the functionality of a DXX node with a combination of Cross-connect, Control and 4x 2Mbit/s G.703 interface units, and one additional interface unit. The additional interface unit can be any type of the DXX standard one slot units, but initially only in RBS2000 verified with one GMH unit supporting two G.704 framed interfaces.

With DXX Manager, the DXX plug-in unit provides enhanced management support in terms of Fault and Performance management . It supports end-to-end circuit provisioning, and network recovery on trunk and circuit level.

It has the following main functions;

- Complete Cross connect wit 4x 2 Mbit/s ports
- One slot with additional 2-4 interfaces
- Support mixed media (LTE, HDSL -copper pairs or OTE -fiber optical cable)
- Switching at nx64 kbit/s and nx8 kbit/s
- Interface for local configuration and supervision
- HDLC channels for connection to DXX Manager
- 1+1 (hot standby) line protection
- Monitoring of synchronisation signal quality
- External synchronisation source for BTS
- Neighbour Node Monitoring and circuit test loops

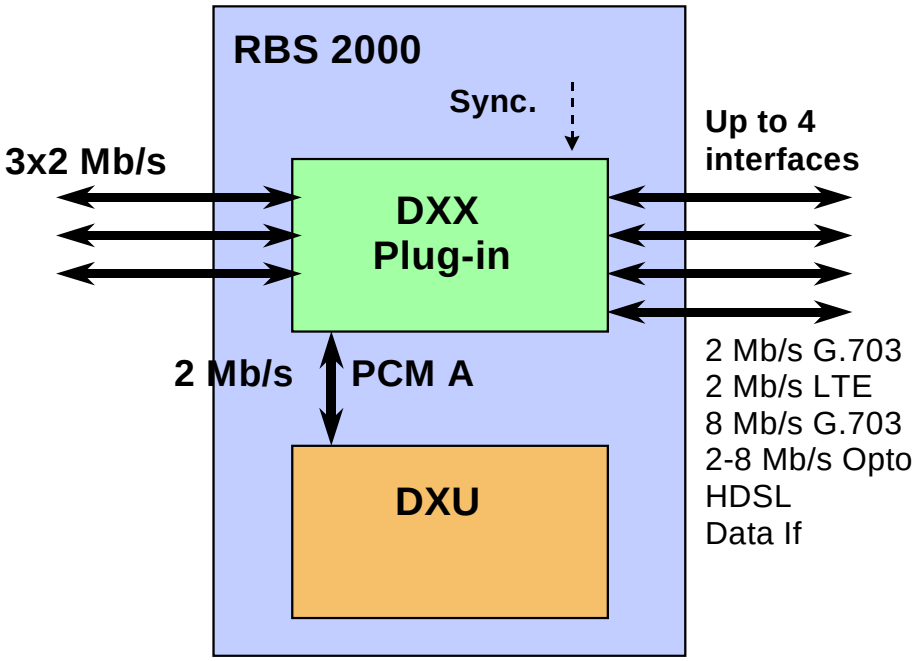


Fig. 1-1. DXX Plug-in unit, 2 Card together with the DXU

The DXX Plug-in unit is in the RBS 2000 interconnected with and housed beside the DXU, and cabled to the connection field of the RBS.

The DXX Plug-in unit is a highly integrated 14T wide unit combining the main functions of a DXX control unit (SCU) and cross-connect unit (SXU-A), and four 2 Mbit/s interfaces (75 ohm or 120 ohm). Additionally one standard DXX unit can be integrated providing more ports or other types of interfaces. The plug-in unit has a back-plane connector that interface to the RBS back plane. The major part of a DXX plug-in unit, 2 card is the housing, the common functionality (multifunctional) unit and the additional interface unit. The unit is from a management point of view regarded as a two slot DXX basic node. The unit has a cross-connection capacity of 64 Mbit/s. It cross-connects n x 64 kbit/s as well as a limited number of n x 8 kbit/s. The unit is designed to operate as a part of DXX-network controlled with Ericsson DXX Network Management System, or can for smaller networks be controlled standalone (with a service computer and unit alarms to BTS). The unit has power and alarm LEDs and an alarm interface towards the RBS.

There are four G.703 2048 kbit/s E1 interfaces, synchronisation input/output and Service Computer interface on the common unit of the DXX plug-in unit. Two of the interfaces (IF 1 and 2) can be used in 1 + 1 protected mode and they support full DXX trunk interface features including management via HDLC channel in any time slots or in the TS0 spare bits. Two interface (IF 3 and 4) do not support management HDLC channel and are intended for connection to the BTS, PCM-A and a co-sited RBS (or the PCM-B). All four interfaces can be used in framed or unframed mode. The frame structure of the interfaces is according to CCITT G.704. The unit front panel houses alarm LEDs for the unit.

The additional unit is optional and provide more functionality to the RBS in terms of number of ports or other type of interfaces than the standard G.703. Initially it supports G.704 framed interfaces at nx64 kbit/s up to 8 Mbit/s, using the DXX GMH unit. Conceptually also data interface, and for example T1 (1.5Mbit/s) can be provided.

The GMH unit processes framed signals at 8448 kbit/s, 2048 kbit/s and n x 64 kbit/s. The unit includes two independent transmission channels to carry data and also to provide an internal communication link of the DXX system. Transmission channel interfaces are independent of each other and they may, for example, be G.703 interfaces, optical interfaces and, at certain rates, also base-band interfaces. The frame structure is in accordance with *G.704* for 2048 kbit/s and 8448 kbit/s. A modified G.704 frame structure is used for other speeds.

The unit front panel houses alarm LEDs and a measurement point (75 ohm) connector. Input and output signals of both channels can be switched to this measurement point. The front panel openings are suited for all available interface modules.

The following interfaces exists for the GMH at present;

- 2 Mbit/s G.703, 75 ohm
- 2 Mbit/s G.703, 120 ohm
- 8 Mbit/s G.703, 75 ohm
- 1-2 Mbit/s G.703 long-haul (LTE)
- 0.5-2 Mbit/s ETSI - HDSL
- 2-8 Mbit/s Fibre optical (OTE)
- Up to 4 Mbit/s Base-band over Copper pairs
- Nx64 kbit/s trunks over V.35/36 or X.21

2. MECHANICAL DESIGN

A DXX plug-in unit consists of the following parts:

- The DXX plug-in card-cage
- The Multifunctional unit (75 or 120 ohm)
- Cable cover

The DXX-plug-in unit can be equipped with

- One optional interface (or server) card

In addition when used in RBS 2000, a set of cables and card guides is required.

- Cable (one) for connection DXU to DXX (75 ohms or 120 ohms)
- Cables (three) for DXX to RBS external cabling (75 ohms or 120 ohms)
- Cables (two to four) for the additional interface card to RBS internal cabling (if the unit is included)
- Alarm cable for TM alarms to BSS (optional)
- Card guides (two) for RBS Sub-rack

Starting from the upper left edge of the front of the DXX plug-in unit card-cage, there are three 'node alarm' LED's, and one power LED. Lower at the front it is an optional cable outlet for Transport Module (TM) alarms (PMA, DMA and MEI). The alarms can be connected to RBS external alarms, in order to supervise the Transport Module when not connected to an DXX MANAGER.

At the top of the always mounted multifunctional unit it is two alarm LED's (for the unit) and a Service Computer connector. Below the SC connector there are two G.703 interfaces, SYNC I/O connectors and again two G.703 interfaces. The traffical and sync. interfaces are D-sub or SMB coaxial depending on if it supports 120 ohm or 75 ohm.

To the left of the multifunctional unit it is a 5T wide standard DXX card position. It can be equipped with any standard DXX unit, but the plug-in unit is in the RBS 2000 initially only verified to support the DXX GMH unit, with two ITU-T G.704 framed interfaces. The unit is intended to provide the RBS with more ports or other type of interfaces like 8 Mbit/s G.703 or fibre optical , 2 Mbit/s long-haul copper or fibre optical interfaces.

The two DXX units and the interface connectors are covered with a cable cover. The cable cover is fixed to the card-cage with two screws. The cover also has the function to lock the optional unit.

In the back of the Plug-in unit it is an Eurocard connector interfacing to the RBS2102/2202. The back connector is only used to get the +24V power supply from the RBS back-plane. The power supply module is mounted in the sub-rack.

The RBS cabinets has no card guides for optional units and those must be mounted in the sub-rack before the DXX unit is plugged in. Cables are provided for interconnection to the DXU and RBS internal cabling.

DXX Plug-in unit - front view

Fig. 2-1 shows the connector locations and the LED's. A 75 ohm coaxial interface and a 120 ohm symmetrical interface for an external clock input and the node clock output have been provided. Both coaxial and symmetrical interface version is available. The coaxial interface is of SMB type and the symmetrical interface is of D-sub connector type.

Fig. 2-1 The DXX plug-in unit, 2 card – Front view

The numbering of the different connectors and interfaces are described in chapter 4.

3. ELECTRICAL AND FUNCTIONAL DESIGN – COMMON PARTS

3.1 BLOCK DIAGRAM

The main block takes care of data and timing signals, the 16896 kHz main clock, frame and multiframe synchronisation's. The external clock reference signal for the main clock can also be connected from any IF as well as from the SYNC interface. The alarm output signals (PMA, DMA, MEI), inventory management, storing parameters for all interfaces and event reporting to the DXX MANAGER are other responsibilities of the main block. The block is not protected.

The functional block diagram is presented below in the figure Fig. 3-1. The common functional blocks are:

- Cross-connect block
- Microprocessor block for control functions
- Power supply
- Interface module G.703-75-4CH or G.703-120-4CH

The microprocessor block, and the cross-connect block, are located on the main board, which is the main board of the unit. The channel interfaces and the sync-interface are located on the interface module.

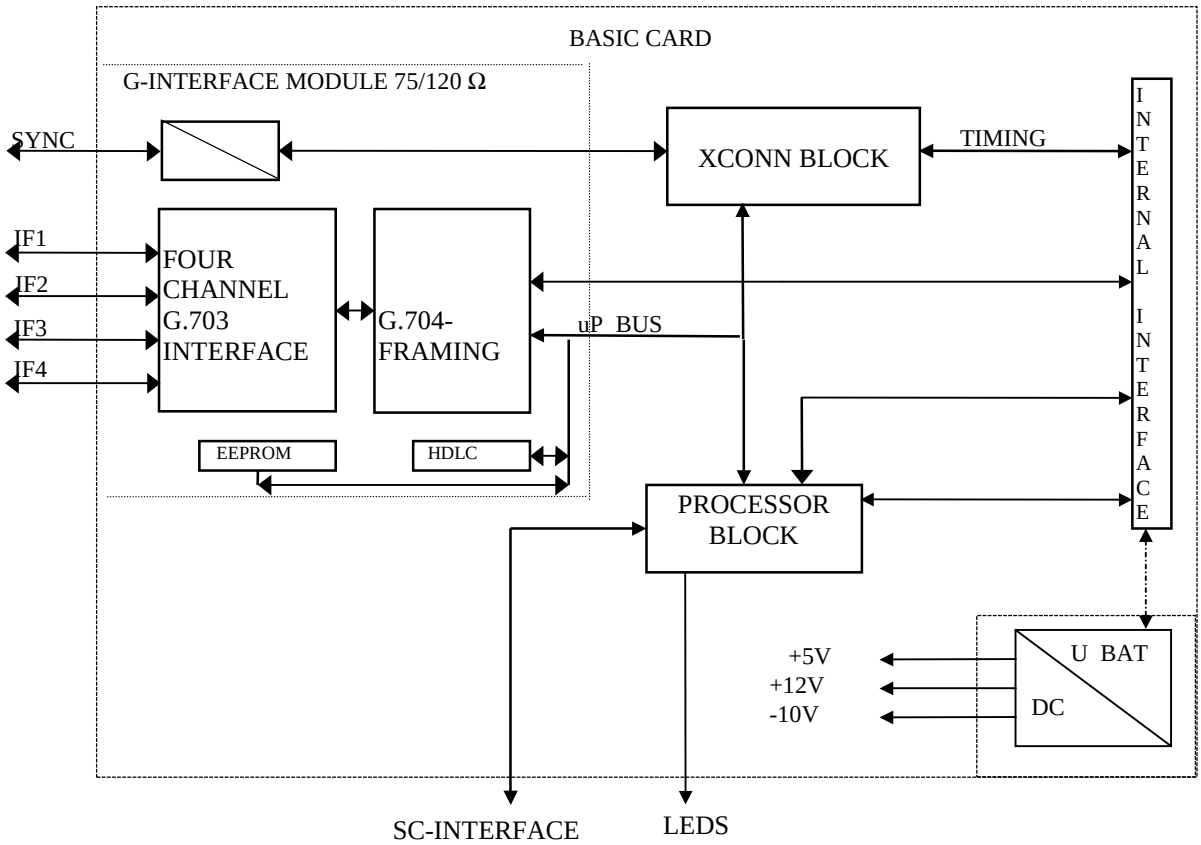


Fig. 3-1 Functional Block Diagram of Plug-in Unit without the optional interface unit

3.1.1 Cross-Connect Block

The cross-connect block has the following main functions:

- cross-connection of data channels
- control of the cross-connect bus
- unit's master clock oscillator
- interface for external clock I/O
- selection of a reference signal for the master clock oscillator
- selection of a clock signal for the external clock output

The cross-connection is done in the switching matrix of the cross-connect block. The cross-connection bus contains 1056 cross-connectable time slots (8-bit bytes). The bits from the interface blocks are collected by using this bus. The cross-connect switch combines the needed new bytes for the interfaces by using 8 kbit/s granularity. Usually, whole time slots or bytes are cross-connected. The delay caused by the cross-connection is one 8 kHz frame (125 µs).

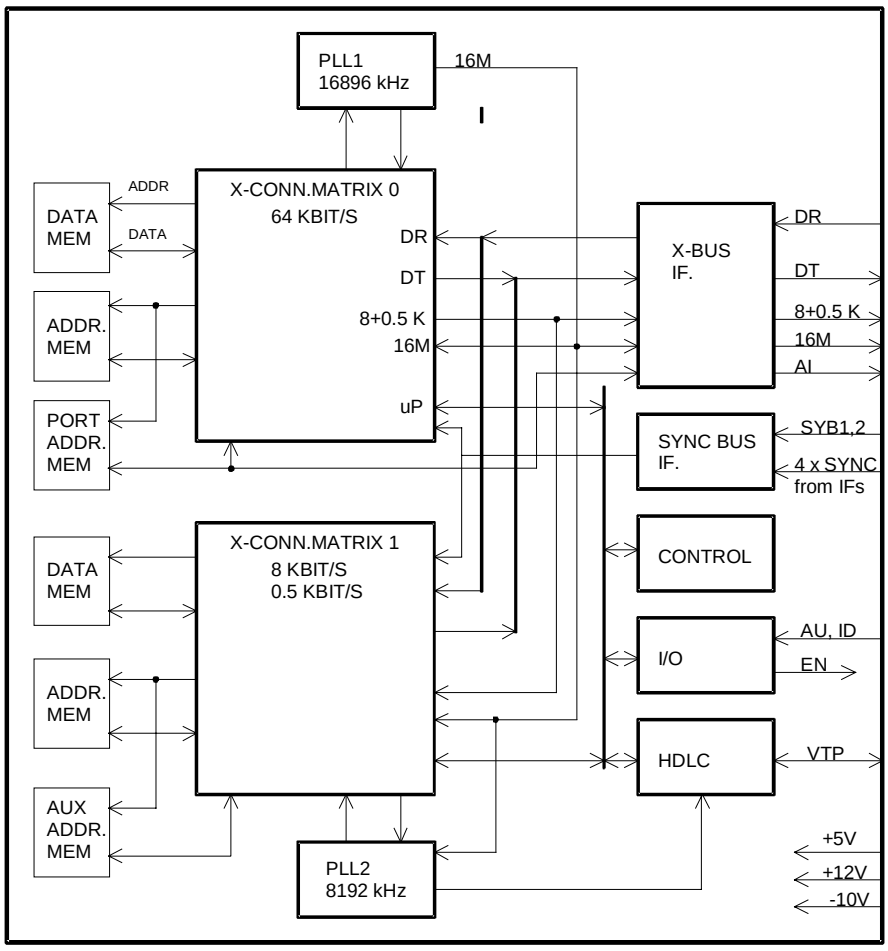


Fig. 3-2 The Block Diagram of XCONN block

The X-connect block exchanges data with IFs or IF-units by placing a channel address on the cross-connection bus, which activates data buffers of the corresponding channel. Rx & Tx data is carried on separate 8-bit buses.

The X-connect block supplies 16896 Mhz master clock signal to the interface module and sub-rack. The Master clock is used to clock the bus operations and to create the correct frequencies for the transmitted signals.

The unit contains two cross-connect matrices (XCM) each handling distinctive connection types. The software assigns tasks to the correct XCM.
Both XCMs enter the signal coming from the DR-bus into a buffer memory. Either of the XCMs outputs an octet in each cross-connected TSB to the DT-bus.

The cross-connect capacity of a Plug-in unit is:

- 1043 x 64 (66 752) kbit/s of n x 64 kbit/s (octet) connections (total capacity).

Out of the total capacity can be allocated:

- 32 x 64 (2048) kbit/s to n x 0.5 kbit/s (channel associated signalling) connections and
- 95 x 64 (6080) kbit/s to n x 8 kbit/s (bit) connections

When calculating the capacity of a connection, add both ends of the connection to the capacity requirement; for example two ports, each requires one 64 kbit/s octet.

Cross-Connect Matrix 0

XCM0 connects all n x 64 kbit/s XB-channels (fully non-blocking).

The DR-bus data is written into the buffer memory, which is two frames long, using an address from the frame counter. Data is read from the buffer with an address, which itself is read from a cross-connect address memory. The unit processor writes this cross-connect address when cross-connections are created.

In each cross-connected tsB a port address and a possible ts-address (framed interfaces) are read from a port address memory. The address is repeated in every frame. Several slow speed access interfaces in the same IF-unit can share a bus time slot, for example eight 8 kbit/s ports one tsB (subrate access interfaces at max. 4.8 kbit/s using a port rate of 8 kbit/s).

A number of ports can share an XD-time slot by using the same port address and activating themselves in only part of the frames.

XCM0 contains frame- and multiframe counters, which supply the X-bus timing. The frame- and multiframe counters of the XCM1 synchronise to the XCM0.

Cross-Connect Matrix 1

XCM1 provides n x 0.5 kbit/s XD-channel and n x 8 kbit/s XB-channel connections. Both types are connected bit-by-bit. Total capacity is 127 time slots (ts) per frame (8128 kbit/s).

Between 0 and 2048 kbit/s can be used for XD-channels (fully non-blocking). In XD-time slots the DR-bus signal is written into a two multiframes long buffer memory.

The maximum capacity for n x 8 kbit/s XB-channels is 95 ts per frame (6080 kbit/s). All ports in a Transport Module (TM) with should be locked as uneven ports. Otherwise there may be blocking in the n x 8 kbit/s capacity.

XCM1 produces one cross-connected byte in every eighth tsB during the frame and transfers the byte temporarily into an internal buffer. All bits in a byte are processed even if some bits are not cross-connected (they are set to idle state '1'). Bytes are read from the internal buffer to the X-bus using addresses from an auxiliary address memory. XD-bytes are read from the buffer in tsB 528 to 559.

3.1.2 Microprocessor Block

The control microprocessor block contains the following functional units:

- Microprocessor
- Memory
- HDLC channel
- A/D conversion
- Service Computer Interface

Microprocessor

The unit is controlled with a 16-bit microprocessor. The processor has access to the cross-connect matrices and the cross-connect memories without interfering with the existing connections. A watchdog monitors the operation of the processor. The system program is stored on the board in two interchangeable EPROM memories. The application programs are stored in non-volatile FLASH memories; it is thus possible to update these programs from DXX Manager. The non-volatile memory is also used to store the unit's operating parameters, the unit serial number, cross connection data info. , port parameters and the parameters of all IF units in the Transport Module (TM). In the case of a power interruption the unit is automatically reset to the conditions prevailing before the interruption, without specific parameterisation. The RAM memory of the processor operates as a working storage containing e.g. error counters and data buffers for the HDLC links and the frame control bus. The microprocessor supports system-level testing.

Memory

The 512 kbyte non-volatile memory is for saving cross-connection data and port parameters as well as program code. Cross-connections can be repeatedly deleted and entered without capacity overflow. The core of the program code is stored in an EPROM. Memory is implemented with surface mount components.

- 256 kBytes RAM
- 512 kBytes Flash memory
- 256 kBytes of EPROM

HDLC Channel

The processor links to the control bus via an HDLC-controller. The main block stores cross-connection commands and port parameters of all interfaces in a non-volatile memory. The unit restores its state should a power loss occur.

A/D Converter

The unit includes a multi-channel analogue-to-digital converter (ADC) which monitors the operating voltages, auxiliary voltages and control voltage of the master oscillator.

Service Computer Interface

The unit has a single asynchronous serial channel. This interface is used on service computer connection (CNF1). The baud rate of the UART is 9600.

3.1.3 Power Supply

The RBS voltage which is used as supply voltage for the power supply module is connected from the RBS back-plane through the card-cage (DXX plug-in unit) rear connector to the two units within the card-cage. The two units has their own individual power module. This module can be replaced as a whole and it is plugged into the unit with connectors. The module is fixed with screws in a place reserved for it on the unit. The module provides the operating voltages +5V, +12V and -10V. The module also receives a +5V bus voltage (from the motherboard of the card-cage), which during start-up conditions is supplied to the interface circuits connected to the internal bus. The operating voltage +5V of the unit is monitored with a reset circuit and a low operating voltage results in unit reset. All operating voltages as well as the +5V bus voltage are monitored by measuring them with an A/D converter. An alarm is generated if a voltage exceeds its limits.

3.1.4 Interface Module

Four-channel G.703 interface module is intended to be used with a base unit. There are two alternatives of the unit, one for a 75 Ω unbalanced interface, G703-75-4CH and another for a 120 Ω balanced interface, G703-120-4CH. The modules include four independent E1 transmission channels to carry data and also to provide an internal communication link of the DXX system. The function of the module is to convert signals received by the base unit of a DXX - RBS plug in unit so that they comply with *G.703* specifications and other relevant recommendations concerning the electrical interface towards equipment outside the DXX network. The G703 module also converts signals from other equipment into signals acceptable to the DXX network. Transmission channel interfaces are independent of each other. The frame structure is in accordance with *G.704* for 2048 kbit/s. Two interfaces can be used for DXX trunk connections with a 1+1 protection possibility and all four interfaces can be used as user access points.

3.2 TRANSMISSION INTERFACES

The common part of the DXX Plug-in unit provides four 2 Mbit/s interfaces. For information of the functionality supported by the interfaces refer to the 2 Mbit/s interfaces described in chapter 4 - Optional interface unit (G.704).

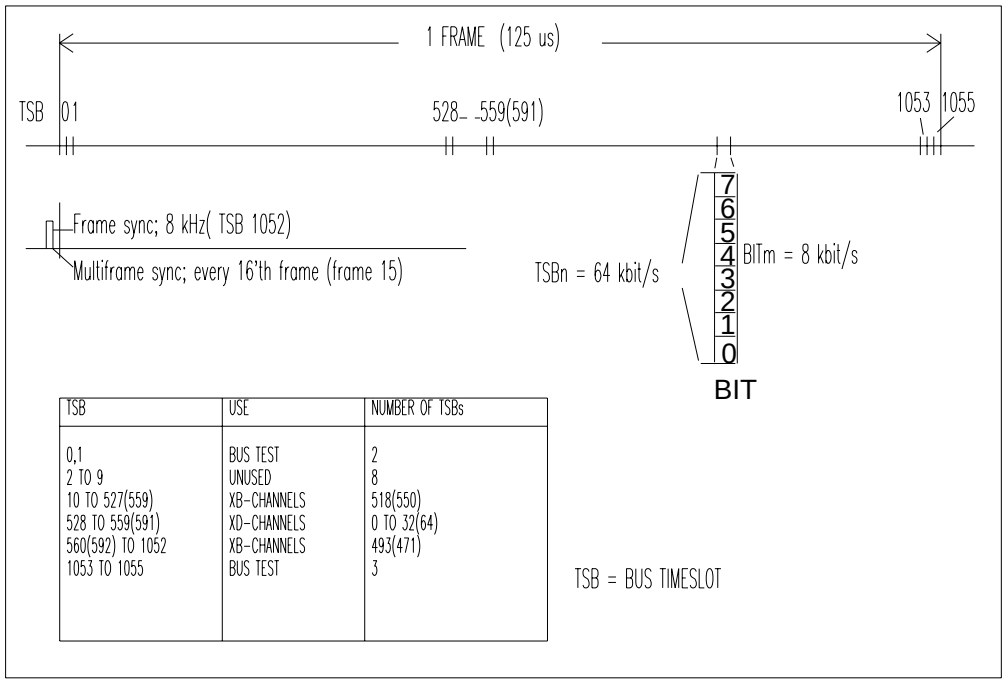
3.3 INTERNAL BUSES

3.3.1 Cross-Connect Bus Structure

The DXX Cross-Connect bus is in the application with DXX plug-in unit only used for internal purposes. The bus is in applications with more units also used between the different units.

When the interface is synchronised and the corresponding cross-connection is made, the unit will activate the **IA Activity Missing** alarm, if it cannot receive its channel address from the internal bus. The interfaces monitor the combined information formed by the bus clock and multiframe synchronisation signal; if this information is missing the interface unit will activate the **Bus Sync Missing** alarm.

The cross-connect block is continuously testing the XCON bus by transmitting test patterns in TS 1053.
The X-bus operates synchronously. The XC block handles the bus clock (16896 kHz), frame timing (8 kHz) and multiframe timing (0.5 kHz).



TSB	USE	NUMBER OF TSBs
0,1	BUS TEST	2
2 TO 9	UNUSED	8
10 TO 527(559)	XB-CHANNELS	518(550)
528 TO 559(591)	XD-CHANNELS	0 TO 32(64)
560(592) TO 1052	XB-CHANNELS	493(471)
1053 TO 1055	BUS TEST	3

Fig. 3-3: Logical Structure of the X-Bus

The X-bus frame is divided into 1056 bus time slots (tsB) numbered from 0 to 1055. Each tsB has a capacity of 64 kbit/s. Each of the eight bits in a tsB can be considered as a separate 8 kbit/s channel. Up to 32 tsBs can be further multiplexed by the 16 frames long multiframe for XD-channel cross-connection. The XD-time slots are cross-connected bit-by-bit creating n x 0.5 kbit/s channels.

Five time slots are reserved for internal unit tests and monitoring. The remaining 1051 bus time slots are reserved for cross-connection of user data.

X-Bus Allocation
X-bus capacity is allocated by the unit software based on selected port parameters. Ports are classified as even and uneven ports. The unit supports uneven allocation. 2048 kbit/s ports get an uneven allocation if receive buffer is 4 or 8 frames. An uneven port does not reserve tsBs for XB-channels until the time slots are cross-connected. A possible XD-time slot is reserved when the port is locked. More than 32 uneven 2048 kbit/s ports can be accommodated in a Transport Module (TM), if part of the time slots are not cross-connected and if the signalling capacity is not limiting.

8 kbit/s XB-Signal Connection
The data exchange on the X-bus is similar to that of the 64 kbit/s signal. A whole byte is always transferred. The unit assembles the byte bit-by-bit during eight consecutive time slots. Bits, which have not been cross-connected, are set to idle state '1'. Signal delay is one frame within the XC.

0.5 kbit/s XD-Signal Connection
The procedure is similar to the 8 kbit/s connection, but here the multiframe structure is employed. The delay in the card is one multiframe (2 ms).

X-Bus Interface
The base unit supplies the C16M bus clock through the X-bus. The C16M clock is also the central clock of the sub-rack in other applications: it is used to create clock frequencies for the transmitted signals. The bus supplies frame alignment and multiframe alignment signals to the frame buffers.

The base unit exchanges data with the interface units by placing a channel address on the X-bus which activates the data buffers of the corresponding channel. Received and transmitted data is carried on separate 8-bit wide buses. From the XC the base units receive the time slot address which directs the bus data transmission to one selected time slot at a time.

Mux/Demux
In digital data transmission it is possible to combine several data transmission channels and to send them on the same transmission line by using frame structures. The frames consist of frame alignment signals sent at regular intervals and data channels located at predefined positions between the alignment signals. The frame alignment signal consists of a defined bit pattern, which the receiver will search for in the received serial data flow. When the receiver finds it, the frame alignment signal is synchronized and therefore able to extract the payload data channels and to map them into desired locations. The frame alignment signals repeated at regular intervals divide the transmitted data into frames which have a defined structure for each transmission speed. In the DXX system the frame repetition frequency is always 8 kHz so that frames of different length, i.e. frames containing a different number of bits, must be used for different transmission speeds. A multiframe is created when several consecutive frames are combined into a frame structure by using a second frame alignment signal which is repeated at a lower frequency. For instance, signalling is transmitted in a multiframe structure containing 16 frames repeated at a frequency of 500 Hz.

A more reliable receiver synchronisation is achieved when a CRC check sum is added to the frame structure. Then it is also possible to monitor the quality of the transmission. The CRC check is made in the transmitting end by dividing the binary value of a data block of a fixed length with a defined number. The division remainder is transmitted in a frame to the receiver, which then performs a corresponding calculation and compares the result with the result received from the line. The transmission of the data block has no errors when the results are equal. If there is a difference in the results, then the received data block contains one or more errors. The CRC check can be made for a data block of one frame, or alternatively, the CRC check is made for a data block consisting of several frames which then form a multiframe structure.

The CRC check sum is used to check the reliability of the synchronisation by counting how many error containing blocks are received within a defined number of consecutive blocks. If the number of faulty blocks exceeds the probability value, there is a great probability that the receiver is synchronised to a wrong position of the frame, i.e. the receiver has made an error in the frame alignment. Then the receiver is forced to make a new search for the frame synchronisation word and to abandon the so called **simulating frame synchronisation word**.

The transmission quality is measured as the error rate by counting the number of received faulty blocks within a given number of blocks. The CRC check sum method is feasible when the transmission error rate is so low that there is maximum one transmission error on the average in a checked block.

The internal communication of the DXX network is based on HDLC channels which are added to the framed signals. The unit processor can transmit and receive messages to/from other DXX Nodes with a two-channel HDLC controller connected to both framed interfaces of the unit. Usually the messages are sent via the control bus to the other units where they are processed or through which they are sent to other DXX nodes. The transmission speed of the HDLC channels can be selected within the limits of 4 kbit/s to 64 kbit/s, depending on the requirements and the available transmission capacity.

In addition to the frame synchronisation words and the transmitted data channels the frame structures also include some bits for which the recommendations have not specified any function or which are not used in the application in question. These bits can then be used for the internal information transmission of the system. A system or organisation can also specify the use of these bits for some internal functions. In the DXX system the function of these special bits is defined through the user interfaces.

3.4 TM CLOCK SYSTEM

The main oscillator (PLL1) runs at a frequency of 16896 kHz. Accuracy in internal timing mode is $\pm$ 30 ppm over the operating temperature range. The main oscillator can be locked to an external source or to the received clock of an access interface.

Auxiliary Oscillator

An auxiliary oscillator (PLL2) is locked to the PLL1 providing frequencies in the 2048 kbit/s hierarchy for the clock output interface. Frequency of oscillation is 8192 kHz. PLL2 also supplies the 2048 kHz clock used for connection to the sub-rack control bus VTP and Tx-clock for interfaces.

Fallback List

In a DXX network, trunk lines are normally used to transfer timing to the Transport Module (TM). While the TM clock can be synchronised from interfaces at lower rates (n x 64 kbit/s) via the external clock interface, it should be noted that synchronisation from 2 Mbit/s signals results in better controlled wander properties.

The operator selects in the Master Clock-menu of the Node-window ports for the fallback list and assigns their priority. Up to five ports can be entered. The unit selects the highest priority port with a non-alarm status as the input to the main oscillator.

Clock Monitoring and Alarms

The unit monitors the clock selected and also the next choice on the fallback list. The external clock is monitored when enabled.

Fallback list clocks are also monitored by the interface units. By a major fault in a port's rx-signal, the IF-unit clamps the clock (on SYNC BUS 1/2) and sends a clock status message to the unit. The units monitoring circuit opens the phase-locked-loop maintaining the clock frequency until the processor selects another clock. Internal timing is selected if all clocks on the fallback list have failed.

2 Mbit/s interfaces with a frame structure can employ a dedicated bit in the frame as a clock far end alarm bit (FEA). It is used on trunks transferring timing between DXX nodes. If an intermediate node in a network loses its synchronisation, the alarm bit is transmitted from all its interfaces. The receiving node’s IF-unit then clamps the clock on sync bus 1/2.

After a fault is cleared the IF-unit gradually clears the clock status. The operator can enter a clock acceptance time in the Master Clock-menu. A clock is not selected again until its status has been good over the acceptance time.

Clock RAI

The unit can employ a dedicated bit of the frame structure as a far-end clock alarm bit. When a node loses the synchronisation with the network, it activates the alarm bit. When the node receiving synchronisation from the faulted node detects the alarm state of this bit, it can cease to use the corrupted clock and select the next clock source from the fallback list.

The DXX Manager is able to select the bit used as a clock RAI. The user must choose a time slot and a bit for the clock RAI. The clock RAI time slot cannot be used for payload data. Special bits like HDLC can, however, be used in the same time slot with the clock RAI. The user must also select the polarity (active state).

The interface activates the clock RAI in the transmitting direction when it receives an alarm message from the cross-connect unit via the control bus. The clock RAI is inactivated in a corresponding manner.

In the Rx direction the clock RAI bit is separated from the incoming data and sampled by the processor with a sampling period of about 10 ms. The state of the bit is preserved when two consecutive equal states are detected. When a unit in the active state receives the clock RAI bit, it will cut off the SYB clock if it has one. If the cross-connect unit loses the SYB clock, it will select the next clock source in the fallback list. If the clock signal is lost for a short period, the interface module returns the clock to the SYB bus when the clock RAI is inactivated and then the cross-connect unit again will use the clock. If the synchronisation is lost for a longer period, the cross-connect unit will remove the faulted interface from the SYB bus by a command through the control bus; thereafter the cross-connect unit directs a command to the next object in the fallback list without an SYB bus to have it connect the clock to the cleared SYB line.

Clock Output Interface

Transport Module (TM) clock output is provided at the external interface in the interface module (G703-75/120-4CH). The output is activated and its frequency selected from the Master clock window. The output control function, when set to on state, disables the output when the unit is in internal timing or locked to the external interface. When output control is off, clock output is active regardless of the fallback list state.

Clock Faults Monitored in the unit

Fault description	Status	Led	Alarm message
All but one clock on fallback list have failed	MEI	-	Fallback list warning
All clocks on fallback list have failed	MEI	-	Loss of master clock locking
External clock on fallback list and missing	MEI	Red	Loss of external clock
External clock on fallback list, clock interface disabled	PMA	-	External clock warning
Locking to a clock failed	PMA	Red	Phase-locked-loop alarm
Main oscillator fault in unit	PMA	Red	X-connect RAM fault
Clock far end alarm (individual for each link)	MEI	Yellow	Clock far end alarm

3.5 TM LEVEL OPERATIONS

The software of the main block takes care of the following node-level operations:

- Node Inventory Management
- Backup of unit settings
- Node alarm (PMA, DMA, MEI) control
- Channel test loops

Node Inventory Management

The Node Inventory Management software includes functions to get and set node and sub-rack identifications, to create and delete inventory, to add and remove units, to get inventory reports and to monitor the presence of registered or unregistered units. The **Create Inventory** operation is used to register all existing units for the inventory. The **Add Unit** operation is used to register a given unit for the inventory. The **Delete Inventory** makes all units unregistered - in other words, all units are removed from the inventory. The **Remove Unit** operation is used to remove a given unit from the inventory.

The **Inventory Report** provides the node and sub-rack identification data and the list of existing or registered units. The **Installation Error** fault condition is detected if the inventory data is not unambiguous and consistent. The **Missing Unit** fault condition is detected if a registered unit is not present. The **Extra Unit** fault condition is detected if there is an unregistered unit present in the sub-rack.

Transport Module Alarm Control

The mani block controls the relay outputs for the node alarms (PMA, DMA, MEI), accessible at the extension unit. The alarms are for optional use when the DXX Manager is not used. The alarms are connected to RBS external alarms, and can be viewed at the BSC location.

The alarms can be delayed. The alarm delay can be set (0…600 seconds) by the user. A summed alarm must be active at least for the set delay time - not necessarily continuously - before the rack alarm is activated in the unit. The alarm will be inactivated in the unit when the summed alarm has been continuously passive for at least the set delay time.

The alarm PMA and DMA can be cancelled. The alarm cancellation is not delayed. When PMA and DMA have been cancelled, MEI is activated as a reminder.

Below is a block diagram is showing the access of the node alarms.

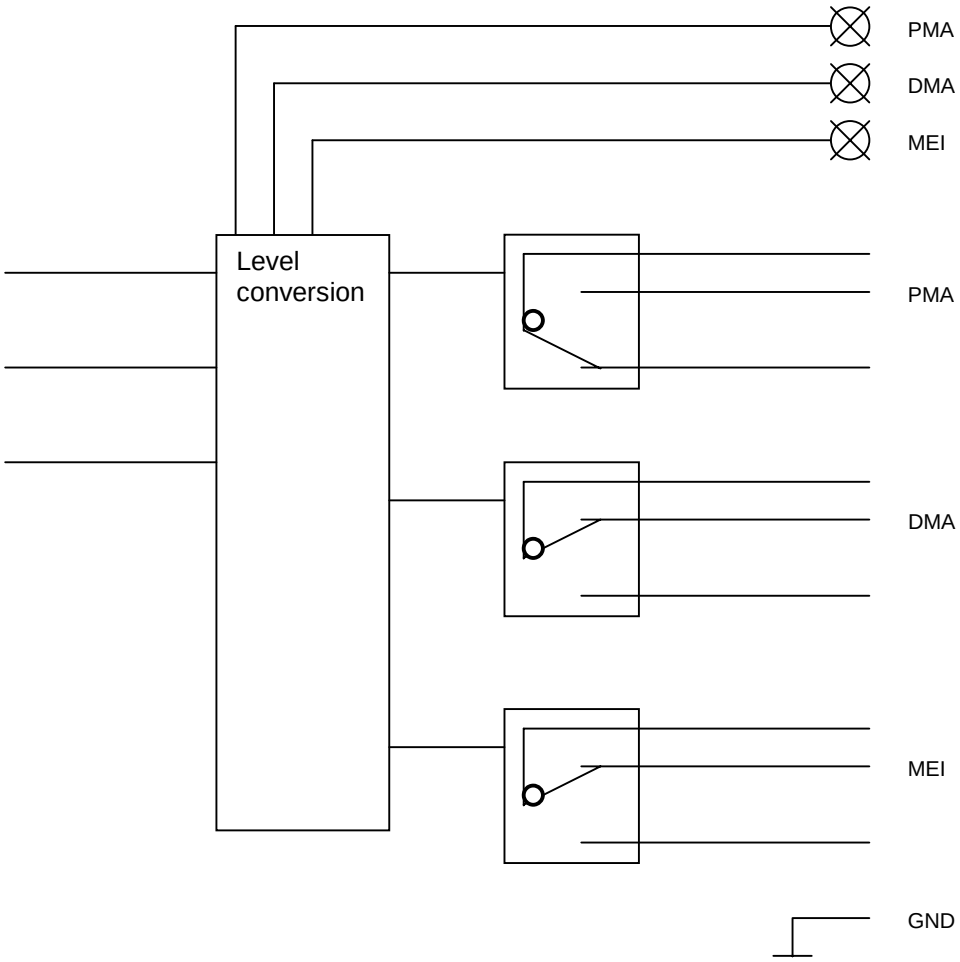


Fig. 3-4: Node Alarms

Connector pinning of the alarm interfaces is described in chapter 6 - unit cabling data.

4 OPTIONAL INTERFACE UNIT

4.1 G.704 FRAMED INTERFACE UNIT (GMH)

The GMH unit processes framed signals at 8448 kbit/s, 2048 kbit/s and n x 64 kbit/s. The unit includes two independent transmission channels to carry data and also to provide an internal communication link of the DXX system. Transmission channel interfaces are independent of each other and they may, for example, be G.703 interfaces, optical interfaces and, at certain rates, also baseband interfaces. The frame structure is in accordance with *G.704* for 2048 kbit/s and 8448 kbit/s. A modified G.704 frame structure is used for other speeds.

Mechanical Design

The mechanical design of the GMH unit is based on the standard DXX system mechanics. The unit can occupy any card slot in the sub-rack; the general recommendations for sub-rack equipping should, however, be followed.

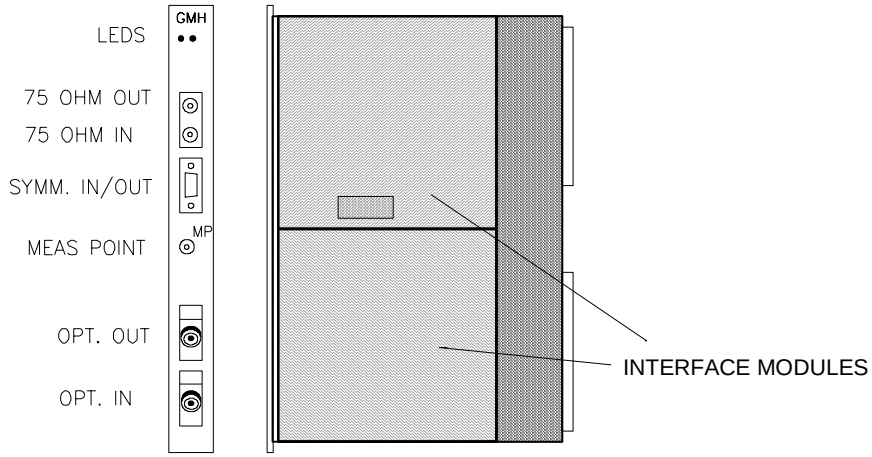


Fig. 4.1-1: GMH Unit Equipped with G703 and OTE-LED Modules

The minimum configuration of the GMH unit consists of a unit power supply module, program memory GMZ 283 and a GMH unit interface module for both channels. The interface modules are selected to suit the particular application in order to provide the physical interface to the transmission line. The two channels can have interface modules of a different type.

The unit front panel houses alarm LEDs and a measurement point (75 ohm) connector. Input and output signals of both channels can be switched to this measurement point. The front panel openings are suited for all available interface modules.

The unit is connected to the DXX sub-rack X bus through connectors at the rear edge of the card. The bus supplies the operating voltage to the unit power supply as well as the signals for the internal sub-rack control bus and for the data transmission processing.

Functional Structure

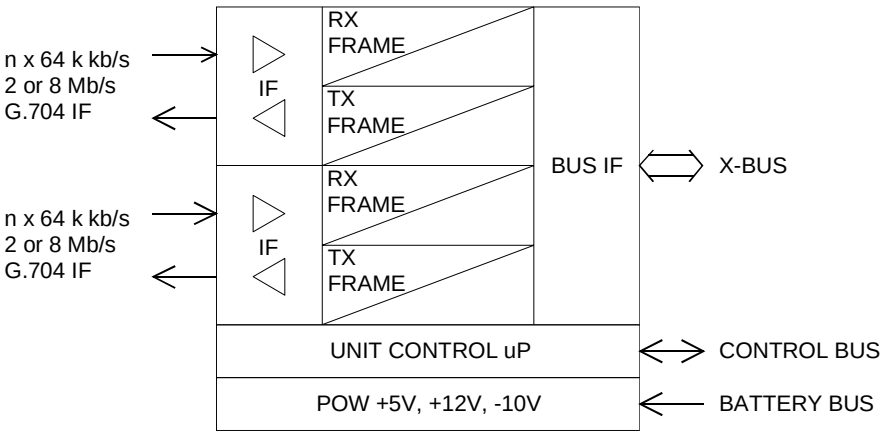


Fig. 4.1-2: Functional Structure of the GMH Unit

The main functional blocks of the GMH unit include the power supply, the processor and its peripheral circuits, line interfaces for both channels, channel frame multiplexer and demultiplexer circuits, channel output and input buffers, and an X-bus interface common for both channels.

The power supply generates the operating voltages required in the unit from the battery voltage it receives from the X-bus. The operating voltages are monitored and a functional disturbance activates a fault message.

The processor with its peripheral circuits controls and monitors the functions of the unit. Information related to control and monitoring is transmitted on an internal control bus of the sub-rack. Through this control bus the unit can communicate with other units in the sub-rack. The processor generates HDLC messages and processes HDLC messages received from framed interfaces.

The data transmission channel interfaces convert analogue line signals to/from signals suited for the unit's digital circuits. In the transmitting direction data pulses are created in a form suitable for transmitting in the required format. In the receiving direction a signal attenuated by the transmission line is regenerated and the clock signal is recovered. The payload signal and the clock signal are transformed to a level suitable for the digital logic. The line interfaces are realised as interface modules so that a unit can have two interface modules of different types at the same time. The available data transmission speeds of the unit depend on which interface modules are used, but the speed can be programmed within the limits of each module.

The framed signal which is carried on the transmission line is assembled and disassembled in the Tx frame and Rx frame blocks of each channel. In the transmitting direction the Tx-frame block creates a signal by mapping data from the X-bus into correct time slots, adding frame alignment signal bits and the CRC check sum, and by generating the HDLC channel at a required position within the frame, with the aid of the processor. In the receiving direction the Rx-frame block searches the received signal for the frame synchronization word. When the synchronization is found, the RX-frame block can extract the data transmission time slots, check the CRC check sum, and recover and supply the HDLC channel to the processor. The frame structure and the use of the special bits in the frame depend on the transmission speed. At 2048 kbit/s and 8448 kbit/s the frame structure is in accordance with *G.704*. A modified G.704 frame structure is used for other speeds. If required, it is also possible to remove the framing and have the channel to operate in a **transparent** mode.

The transmit buffers of the channels are used to store data received from the cross-connect through the X-bus, so that there is always a time slot available for transmit by the Tx frame block. The transmit buffers also synchronize the phase of the transmitted frame with the phase of the X-bus and stuff idle data in unused time slots of the frame.

The receiving buffers of the channels store incoming data so that the required time slots are always available to the cross-connect unit. These buffers also form a flexible buffer in order to compensate for minor momentary speed differences between the X-bus and the received signal. The length of the receiving buffers can be changed in accordance with the application's requirements. For instance, in some cases a minimum connection delay is required, and in plesiochronous operation slips are desired to occur as seldom as possible.

The X-bus interface adapts the bus to the unit. It transfers signals from the bus to the channels, timing signals and control information to the unit, and correspondingly it transfers data and monitoring information from the channels to the X-bus. The bus interface prevents the unit from interfering with the bus functions when the unit is inserted into the sub-rack slot, or when it is removed from the sub-rack, and also if the unit fails.

Unit Operation

Power Supply
A unit receives its operating voltage from the power supply module PDF 202 or PDF 209. This module can be replaced as a whole and it is plugged into the unit with connectors. The module is fixed with screws in a place reserved for it on the unit. The battery voltage which is used as supply voltage for the power supply module is connected from the DXX-bus through the bus connector. The module provides the operating voltages +5V, +12V and -10V. The module also receives a +5V bus voltage, which during start-up conditions is supplied to the interface circuits connected to the bus. The operating voltage +5V of the unit is monitored with a reset circuit and a low operating voltage results in unit reset. All operating voltages as well as the +5V bus voltage are monitored by measuring them with an A/D converter. An alarm is generated if a voltage exceeds its limits.

Processor
The unit is controlled with an 80C188 microprocessor. The program is stored on the board in an interchangeable EPROM memory identified as GMZ 283. A part of the application programs are stored in a non-volatile FLASH memory and thus it is possible to update these programs without removing the unit from its operating environment. A non-volatile memory is also used to store the unit's operating parameters and the unit number so that in the case of a power interruption the unit is automatically reset to the conditions prevailing before the interruption, without specific parametrization. The RAM memory of the processor operates as a working storage containing i.e. error counters and data buffers for the HDLC-links and the frame control bus.

Control Bus
The unit communicates with other units in the sub-rack via the sub-rack control bus. Each unit position in the sub-rack has an individual address which is registered by the unit when it is inserted into the sub-rack. This address identifies the unit during communication. The unit settings can be changed through the control bus with the aid of a service computer connected to the SCU unit. The units are also monitored and fault data is collected through the control bus. Each unit can transmit messages on the control bus when there is no other traffic on the bus. When a unit is transmitting it sends a clock signal and data to the bus. The unit uses the same lines to receive messages from other units. The control bus is secured by having a double bus, the duplication controlled by the SCU unit.

A/D Converter
The unit includes a multichannel analogue to digital converter (A/D) which monitors the operating voltages and also the control voltage from the interface module connectors. The control voltage is. for instance, a voltage received from a baseband module which controls the baseband line power-off situation.

Measuring Point

A 75Ωcoaxial cable measuring point is provided on the front plate of the unit. The measuring point is isolated with a transformer, but the connector body is connected to the unit ground. Through the measuring point it is possible to measure the input and output signals of both channels as well as the corresponding clocks. The signal to be measured is selected with the service computer in the **General Unit Parameters** window. This selection is stored into the unit's non-volatile memory so that the selection is retained also after a possible power interruption.

When measuring the output or input signal of the channel, the output signal of the measuring point is HDB3 coded and the signal levels and formats are in accordance with *G.703*. HDB3 coded channel interface signals can be measured without any coding/decoding. If the measured channel interface signal is coded in another code, then the measuring point coder is automatically used to transform the NRZ signal into an HDB3 signal.

Module Interfaces

A unit is connected to a transmission line through interface modules. The interface modules contain the analogue components required for the interface and also the analogue components needed to generate input and output clocks. The signals between the unit and the interface module are digital signals which are converted to the transmission line level in the module. Line codes are coded/decoded in the unit when modules of G.703 type or optical modules are used; in baseband modules the line coding is performed in the module. Each module type supports defined transmission speeds which can be selected with the service computer. The codes and the available transmission speeds are described in the functional description of the respective units.
The processor bus is connected to both interface module connectors. Through this bus it is possible to detect the module type and to read data regarding the module status, regarding a missing incoming signal, for example. Parameters which define the module functions, e.g. the transmission speed and possible looping commands, can be selected through the bus.

In the receiving direction the interface module regenerates the coded signal received from the transmission line and transforms the signal to the digital level. The module monitors the level of the received signal; if it is too low or completely missing, the module sets an AIS signal to the unit and at the same time it activates a missing signal alarm through the processor bus.

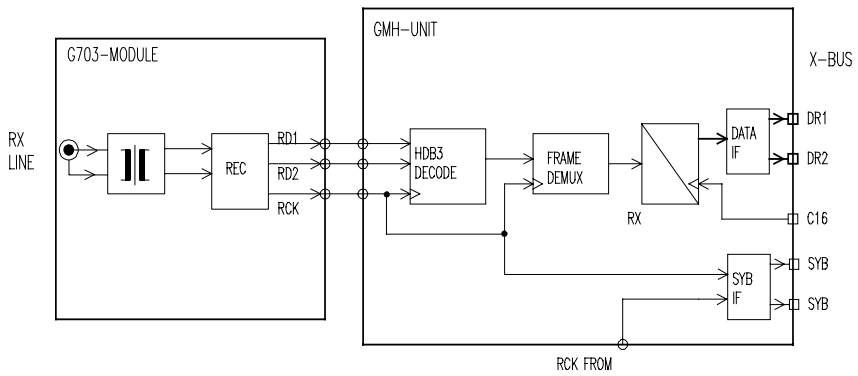


Fig. 4.1-3: Data and Clock Processing in the Receiving Direction

The receiving direction clock is recovered from the data in the interface module. The clock is supplied to the unit, which uses it to decode the line code and to demultiplex the frame. If there is no received signal, the interface module replaces the received clock with the transmitted clock. The receive clock in the V series modules is got from circuit 113 from line. The alarm of missing signal with V series modules is based on detecting the incoming clock signal.

The received clock from both channels is connected to the SYB interface, where the processor can select a desired clock for either SYB-bus to be used as the frame synchronization signal. The clock to the SYB-bus is disconnected if there is a received signal failure.

The unit generates the frame structure for the data in the transmitting direction. The line code of the data is generated in the unit for G.703 interfaces and for optical interfaces. The coded digital data is connected to the interface module, where it is converted to a line level signal. NRZ data for baseband interfaces is connected to the interface module, where it is coded and transformed into a line level signal.

The transmitting direction clock generation depends on the interface module and the transmission speed. In all cases the transmitting direction clock is phase-locked to the C16M frame clock received from the X-bus.

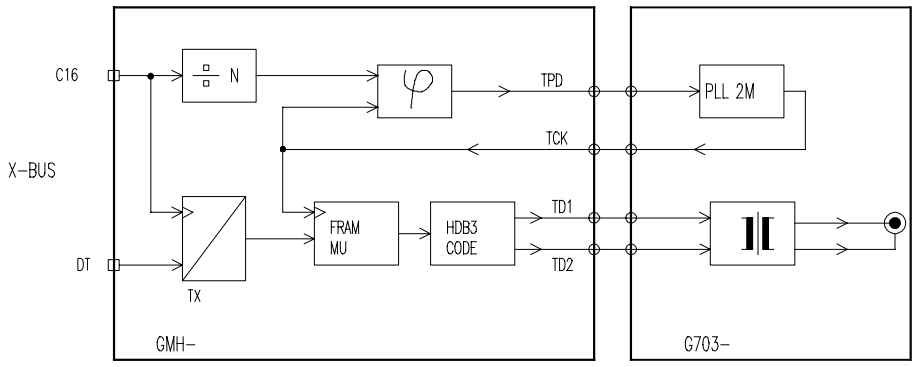


Fig. 4.1-4: Transmitting Direction Clock and Data Generation at 2048 kbit/s

The transmitting direction clock for 2048 kbit/s and 1088 kbit/s is generated by the phase-locked crystal oscillator of the interface module. The oscillator is locked to the C16M clock of the bus, which is used to create the frame and to generate the output pulses in the coder.

Even if the C16M clock is missing, the output signal is generated with the aid of the clock signal from the interface module crystal oscillator. The phase-locked oscillator will then adjust to its nominal frequency and time slot data in the frame is set to AIS.

Mux/Demux

In digital data transmission it is possible to combine several data transmission channels and to send them on the same transmission line by using frame structures. The frames consist of frame alignment signals sent at regular intervals and data channels located at predefined positions between the alignment signals. The frame alignment signal consists of a defined bit pattern, which the receiver will search for in the received serial data flow. When the receiver finds it, the frame alignment signal is synchronized and therefore able to extract the payload data channels and to map them into desired locations. The frame alignment signals repeated at regular intervals divide the transmitted data into frames which have a defined structure for each transmission speed. In the DXX system the frame repetition frequency is always 8 kHz so that frames of different length, i.e. frames containing a different number of bits, must be used for different transmission speeds. A multiframe is created when several consecutive frames are combined into a frame structure by using a second frame alignment signal which is repeated at a lower frequency. For instance, signalling is transmitted in a multiframe structure containing 16 frames repeated at a frequency of 500 Hz.

A more reliable receiver synchronization is achieved when a CRC check sum is added to the frame structure. Then it is also possible to monitor the quality of the transmission. The CRC check is made in the transmitting end by dividing the binary value of a data block of a fixed length with a defined number. The division remainder is transmitted in a frame to the receiver, which then performs a corresponding calculation and compares the result with the result received from the line. The transmission of the data block has no errors when the results are equal. If there is a difference in the results, then the received data block contains one or more errors. The CRC check can be made for a data block of one frame, or alternatively, the CRC check is made for a data block consisting of several frames which then form a multiframe structure.

The CRC check sum is used to check the reliability of the synchronization by counting how many error containing blocks are received within a defined number of consecutive blocks. If the number of faulty blocks exceeds the probability value, there is a great probability that the receiver is synchronized to a wrong position of the frame, i.e. the receiver has made an error in the frame alignment. Then the receiver is forced to make a new search for the frame synchronization word and to abandon the so called **simulating frame synchronization word**.

The transmission quality is measured as the error rate by counting the number of received faulty blocks within a given number of blocks. The CRC check sum method is feasible when the transmission error rate is so low that there is maximum one transmission error on the average in a checked block.

The internal communication of the DXX network is based on HDLC channels which are added to the framed signals. The unit processor can transmit and receive messages to/from other nodes with a two-channel HDLC controller connected to both framed interfaces of the unit. Usually the messages are sent via the control bus to the other units where they are processed or through which they are sent to other nodes. The transmission speed of the HDLC channels can be selected within the limits of 4 kbit/s to 64 kbit/s, depending on the requirements and the available transmission capacity.

In addition to the frame synchronization words and the transmitted data channels the frame structures also include some bits for which the recommendations have not specified any function or which are not used in the application in question. These bits can then be used for the internal information transmission of the system. A system or organisation can also specify the use of these bits for some internal functions. In the DXX system the function of these special bits is defined through the user interfaces.
The frame structures and buffer handling are described in the appendix 1.

4.1.1 OPERATING MODES

The operating modes for 2 Mbit/s described for the optional G.704 framed interface unit is valid also for the interfaces on the common unit described earlier.

GMH Operating Modes

Trunk interfaces and **user access interfaces** are the two categories of DXX node interfaces. Trunk lines are lines connecting the DXX nodes, and the trunks are always framed interfaces. User access interfaces connect lines from users to a node. The user access interfaces can be channel interfaces or framed channel interfaces. GMH units can be used as trunk interfaces or user access interfaces. The user interface presents a G.704 framed channel interface to the user. The most important difference between the trunk mode and the user mode is that the use of time slots in the trunk interface is determined by the Network Management System whereas the use of time slots in a framed channel interface is determined by the user.

GMH Unit as a Trunk

2048 kbit/s Trunk

When a line is used as a trunk line, a part of the frame is dedicated to transfer internal system information. This information will contain data on e.g. network management channels that use the HDLC format. The transmitter will always regenerate the frame synchronization word and the CRC check in a trunk line.

The framing and CRC check have to be selected when a trunk line connection is established. The corresponding HDLC channel has to be activated and bits B5…B8 in time slot ts0 are recommended bits for the link. The trunk buffer is short in order to ensure minimal delay trough the node. It is recommended to activate the signalling time slot CAS of the trunk so that it is always reserved for signalling and not used as a data time slot by the Network Management System.

Split Trunk Lines

A split trunk line can be used to combine several parallel n x 64 kbit/s or 2048 kbit/s interfaces in order to increase the maximum number of time slots of a n x 64 kbit/s trunk interface. The time integrity of the time slots in the split trunk line is preserved even if the n x 64 kbit/s is connected through physically separated cables. The split trunk mode can be used for line speeds n x 64 kbit/s and 2048 kbit/s when a frame with CRC4 is used. The split trunk mode always requires long buffers (eight frames). One of the interfaces will function as a master and the others as slaves. All split components must have same bit rate.

The interfaces are synchronized to each other by their CRC4 multiframe structure. In the transmitting direction the interface transmit buffers and Tx frame multiplexers are synchronized with the X-bus MSYN signal to transmit in the same multiframe phase. In the receiving direction the master interface sends information about its receiving buffer read phase to the slaves, which will center their own receiving buffers to the same phase. This operation causes data time slots sent from a transmitting node in the same frame to be read together within one frame into the SXU unit of the receiving node.

Theoretically, the maximum delay allowed between lines in a split trunk line is 0.5 frames: due to the centring the master read address occurs when the write address is in the area 6…2. Due to technical reasons, however, the maximum delay is 50 μs.

Each line of a split trunk line will handle its own signalling data. Those lines which carry one or more data channels with signalling data will use the last time slot or ts16 if it is possible as a signalling channel with a multiframe structure. It is not necessary to use a CAS time slot for lines that do not include data channels with signalling.

GMH as User Access Point

The GMH unit can provide a G.704 framed channel interface to the user. The framed user access point has the same features as a corresponding trunk interface. The special bits are used in accordance with customer requirements. There are many possibilities to use the GMH unit as a user access point. Some examples are discussed below.

Framed; With or Without CRC

This is the basic way to connect pieces of equipment which use the G.704 frame structure to a DXX node. Only the data channels in time slots ts1…ts31 is transmitted over the network together with signalling data in the time slot ts16, if required.

The framing structure is demultiplexed at the interface point and only payload data will be supplied to the cross-connect system for further processing. In the transmitting direction the whole framing structure and the frame synchronization word are created in the interface and payload data from the cross-connect is added to the frame. The user equipment to be connected has usually no information about the protocol of the DXX system control channel. Therefore the HDLC channel will not be connected to the interface (with the exception of some DXX system modems). The free bits in time slot ts0 can be set to a state required by the user equipment. The synchronization remote end alarm indication bit RAI may be used, if required by the equipment to be connected. It is recommended to use the CRC check in the interface when the user equipment supports the use of CRC. Some equipment use the CRC E bits in a way not conforming to standards and in such cases unnecessary alarms can be avoided by setting the bits in a fixed state, usually 1.

When individual channel signalling is used, the multiframe structure in the receiving direction is demultiplexed in the interface and the signalling for each channel is transferred to the cross-connect for further processing. In the transmitting direction the multiframe synchronization time slot is created in the interface and stuffed with free bits. Signalling data from the cross-connect is placed into the signalling time slot. The free bits usually have the Permanent 1 state. If no signalling is used, then also time slot ts16 may be used to transmit payload data.

Framed; Transmission of Free Bits in ts0 Through the Network

It is possible to transmit the free bits of time slot ts0 through the DXX network when the equipment connected to a DXX node can utilise these free bits. Other functions may be the same as in the previous example. The free bits of time slot ts0, which are utilised by the application and transmitted through the network, are set to the **X-conn** state when the GMH unit parameters are defined. The unit will then transmit these bits in the same state as it receives them from the cross-connect. Accordingly, bits received in time slot ts0 are supplied to the cross-connect in the same state as they are received.

On the transmission line the data transmission capacity is 4 kbit/s for one free bit in time slot ts0 due to the frame alternation. The total data transmission capacity of all five bits B4…B8 is thus 20 kbit/s. However, the DXX system utilizes a format where one free bit of time slot ts0 uses a capacity of 8 kbit/s on those connections on which it is transmitted through the network. Thus, a total capacity of 40 kbit/s is required to transmit all bits B4…B8 through the network. Transmission of the free bits of time slot ts0 always uses 64 kbit/s of the DXX node internal X-bus capacity for each interface, regardless of the number of transmitted bits.

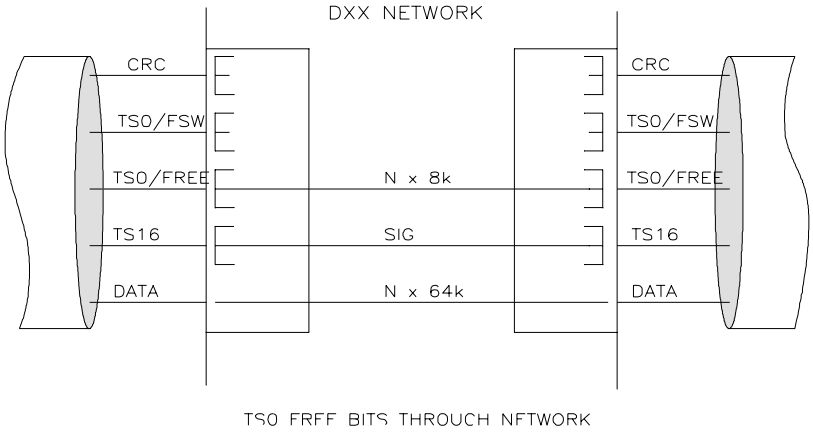


Fig. 4.1-5: TS0 Free Bits Connected Through the Network

Framed; Transmission of Time Slot ts0 Through the Network

It is possible to use the frame synchronization word to monitor the complete connection through the DXX network. In this case the whole time slot ts0 is directed via the cross-connect and transmitted to the far-end equipment. In this case the frame synchronization word, the free bits of time slot ts0 and the frame remote end alarm are transmitted over the whole connection. If it is required to connect signalling data separately over this connection, then the CRC check has to be regenerated in the user access interface. A new CRC check sum has to be calculated because the frame contents will change due to the different treatment of signalling data and normal data. The CRC check may be inactivated when the user equipment does not support the use of CRC.

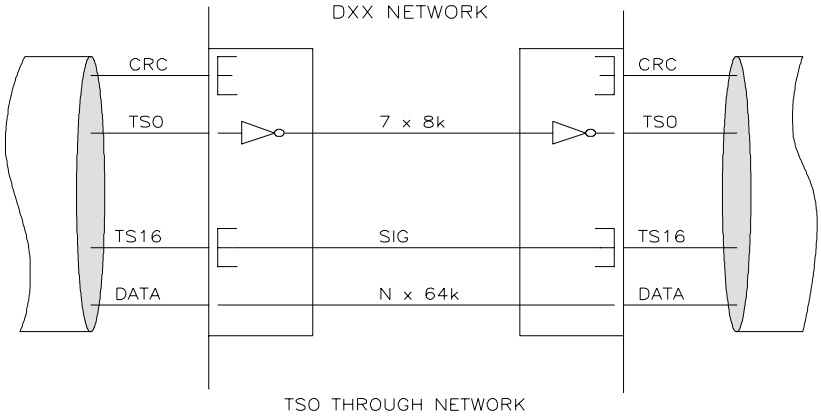


Fig. 4.1-6: Ts0 Connected Through the Network

When it is connected to the transmission network, the time slot ts0 is inverted in the receiver before it is forwarded to the cross-connect. The time slot is in the inverted state when it is transmitted through the network, and in the far-end user access interface it is again inverted into its original format and then added to the frame as the synchronization time slot. The time slot ts0 is inverted so that it cannot cause false synchronization of the trunks when it propagates through the network. A trunk capacity of 56 kbit/s is used in order to transmit the whole time slot ts0 through the network. The transmission of the time slot ts0 uses 64 kbit/s of DXX node internal X-bus capacity for each interface.

When the interface parameters are set (during commissioning), the **Fault consequence BER 10E-3** should be set **Off**. This causes received data with a bit error rate worse than 10E-3 (calculated with the aid of the frame synchronization word) to be connected through the network, and not to be set AIS as in normal transmission.

When the time slot ts0 is transmitted through the network, he user access interface will respond to errors in a way that is different from the normal. The remote end frame level alarm bit is not activated when the user access interface receiver detects a serious frame error, because this error will cause the remote end user equipment to respond, e.g. through the AIS, and to activate the remote end alarm bit. The remote end alarm bit is then transmitted back to the near-nd user equipment. Moreover, the GMH unit will not respond to a received FrFEA bit. If an interruption occurs in the transmission network and an AIS is given instead of a payload signal to the interface, then this condition will be detected in the transmitter and an AIS is sent to the user equipment. The interface simultaneously activates the **AIS from X-bus** alarm.

Framed; Ts0 and CRC Connected Through the Network

It is possible to monitor the quality of the user's connection over the whole network with the aid of the CRC check. To enable this, a combination of the time slot ts0 and the CRC check is sent through the network from the near-end user equipment to the far-end user equipment. The CRC check sum is calculated for the total signal. In order to get equal results in the unit creating the CRC check sum and in the unit evaluating the CRC check sum, all bits must have the same state at both locations. The receiver will receive signalling data and payload data through different delays, and therefore it is not possible to use cross connected channel signalling, if the CRC check is transmitted over the connection. The idle data of possibly unused time slots has to be the same at both ends of the connection.

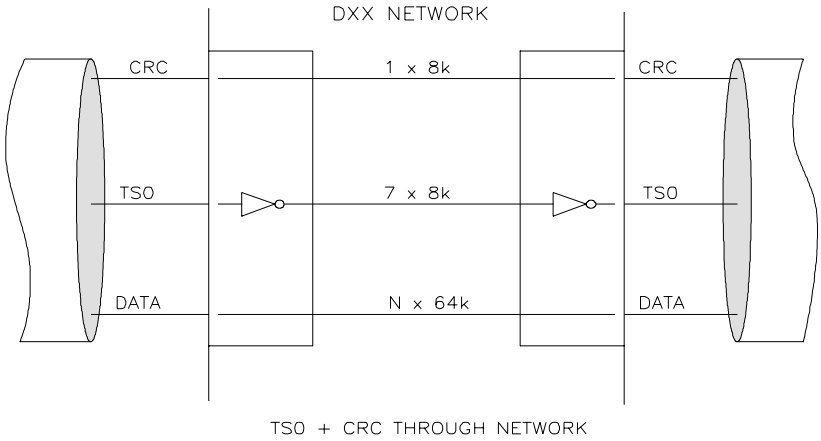


Fig. 4.1-7: Ts0 and CRC Connected Through the Network

The time slot ts0 is inverted before it is transferred to the transmission network. A capacity of 64 kbit/s is used on a trunk line to transmit the combination of time slot ts0 and the CRC check, and 64 kbit/s of the internal DXX node cross-connect bus. CRC check E-bits indicating remote end block errors are also connected through the network. If these bits are not used they must set to the state **1**. The interface responds to errors in the same way as when only time slot ts0 is connected through the network.

Transparent Without Frame

The interfaces of a GMH unit can also operate in a transparent mode. In this mode the received signal is connected through the network without any manipulations. The receiver is not synchronized to the incoming signal frame structure; no additions to the output signal are made in the transmitter. However, the receiver does cut the signal into slices of eight bits, which are transmitted through the network and from these slices a signal conforming to the original signal is then reconstructed in the receiver. In the transmission network a transparent signal requires a capacity according to its interface bit speed.

In order to use the interface in the transparent mode the interface parameter **Framing** must be set **Off** during parametrization. No frame errors are detected in the transparent mode, as the frames are not processed in any way. An alarm for error rate 10E-3 will be calculated only from code errors, whereas the error rate in a normal mode is calculated using also frame synchronization word errors.

Transparent With CRC Monitoring

The interface can be set to a function mode, in which the signal is transparently connected through the network, but in which the user access interface receiver synchronizes to the received signal frame structure and performs a CRC check on the signal. In the transmit direction the signal contents is not changed. The interface is set into this mode by defining the **Framing** parameter as **CRC monitor** during parametrization. The interface will also output framing error information, but actions on these errors are prevented.

In forced operating mode the switch is forced to switch over without delay. Received data from the active interface is immediately connected to the X-bus. In this situation the **Protection switch forced** fault message with status MEI appears, and the red LED is turned on.

A switch operating time delay is defined for the prefer operating mode and the normal operating mode. The delay is defined as n x 10 ms, where n=0…6000; i.e. the delay is 0…1 minutes. The delay defines the allowed fault duration before the switch is triggered to switch over.

1+1 line protection

Interfaces 1 and 2 can be 1+1 protected by each other. In protected mode both channels must have the same speed and framing mode settings. A unit working in the protected mode will look like a cross-connect port towards the X-bus. In the protected mode both channels transmit the same data signal coming from a buffer. Both channels use their own frame mux to create the frame structure. The receiving direction includes a change-over switch that selects the active receiver. Rx signal faults are classified into several categories. The switch uses fault categories to select the interface to be used. The fault categories are indicated in the fault table (see chapter 5). For example **1.x** means the first category (the worst or the most serious fault).

The operating modes of the change-over switch are:

- normal operation
- preferred operation
- forced operation

In the normal operating mode the switch will automatically switch to the other interface if the Rx signal fault category (1, 2, 3, 4, 5, OK) of the active interface continuously is worse than the fault category of the other interface, for a longer period than the given time delay. No switchover operation is activated when the categories are equal for both interfaces.

In the preferred operating mode a switch-over is triggered if there is a difference between the interface fault categories; the better interface is switched active. In a situation with equal fault categories for both interfaces the switch selects the preferred interface.

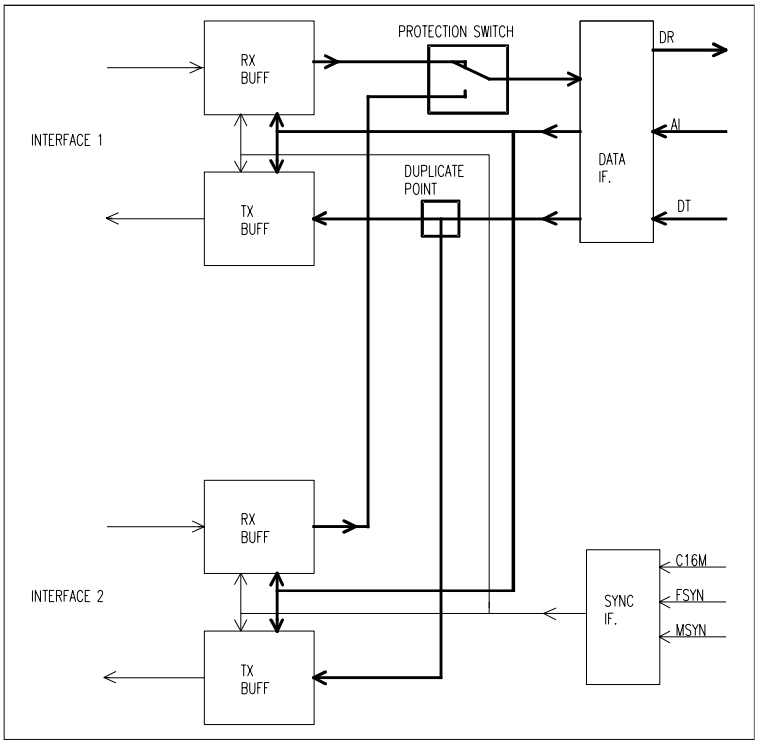


Fig. 4.1-8: Block Diagram of Protection

Fault and Service Status (PMA, DMA, MEI, S) in 1+1 Mode
In principle both interfaces generate their own alarms (alarm messages with fault status). PMA and S statuses are processed in this mode.

PMA Status Processing:
In the protection mode the normal PMA status is changed to the DMA status and there is an additional fault condition, **Loss of protected signal**, with a PMA status. In normal or prefer operating modes this special condition is created when both interfaces have a fault with fault category 3 or worse. In the forced operating mode this condition occurs if the forced interface has a fault with fault category 3 through 1. The inactive interface is not able to generate a fault with the PMA status.

S Status Processing:
In the protection mode an S status is generated only in the **Loss of protected signal** fault condition.

Far-End Alarms in 1+1 Mode
A far-end alarm indicates that the Rx signal is out of service (S status)
FrFEA = Rx frame out of service
MFrFEA = Rx multiframe out of service

Tx far-end alarms (FrFEA, MFrFEA) of both interfaces are generated assuming a fault status of the active interface. During a short period, when the change-over switch is in a transition phase, the far-end may generate an alarm even if there is no fault in the better interface. In forced operating mode only the active forced interface can cause far-end alarms to be sent.

RxAIS Processing
RxAIS and RxAIS to SigTS are always generated when FAE or MFrFAE is sent. AIS generating depends on the fault status of the selected interface.

Terminology:

Maintenance Status:

PMA	=	Prompt Maintenance Alarm
DMA	=	Deferred Maintenance Alarm
MEI	=	Maintenance Event Information

Service Status:

S	=	Service Alarm

LED Indications:

R	=	Red alarm LED
Y	=	Yellow alarm LED
RB	=	Red alarm LED blink

Consequent Actions:

TxAIS	=	AIS insertion to Tx signal
RxAIS	=	AIS insertion to Rx signal
TxTS-AIS	=	AIS insertion in time slots of Tx signal
FrFEA	=	Frame level far-end alarm (ts0/B3 in 2Mbit/s frame, ta66/B7 in 8 Mbit/s frame)
MFrFEA	=	Multiframe level far-end alarm (FR0/ta sig/B6)

MFrFEA is also transmitted if FrFEA is transmitted.

Loops in GMH

The DXX Manager is able to control several loops in the GMH unit. Loops and measurement points are used to find a faulty section of the line and to detect the faulty transmitting or receiving direction. The unit includes a loop time-out control which will turn off a loop when the user defined time has come to an end.

Interface Loop

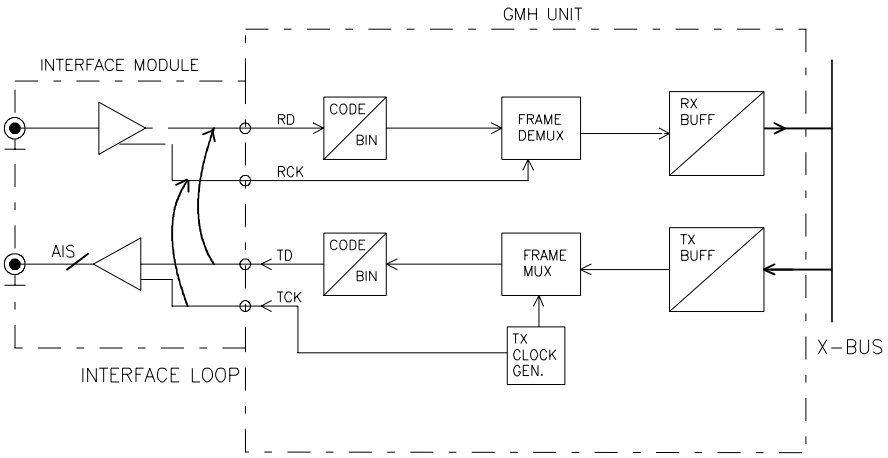


Fig. 4.1-9: Interface Loop

An interface loop is created in the interface module. It loops the transmit data and the clock signal back to the interface receiver. AIS is sent from the interface and the yellow alarm LED is switched on.

The type of the module determines the point where the loop is created in the module. In most cases, due to technical reasons, the loop is not made using a signal with line level. The loop will, however, always test the interface module control bus and connectors and a part of the module logic. The line coder and decoder as well as the frame multiplexer and demultiplexer are also tested in the loop. There should be no other faults in the unit's fault list when the loop is created.

Equipment Loop

In an equipment loop the transmit data from the G.704 multiplexer before the interface module is looped back to the demultiplexer. The interface sends an AIS and the yellow alarm LED is switched on.

The equipment loop is made in the unit. This loop tests the frame multiplexer and demultiplexer. Neither the line coder/decoder nor the interface module are included in the loop. It is also possible to detect faults in the transmitting and receiving buffers when a test signal from a measurement equipment is added to the signal passing through the looped channel. If no problems are detected with the interface loop, it is suggested to perform a test with the equipment loop to ensure that the module is in order.

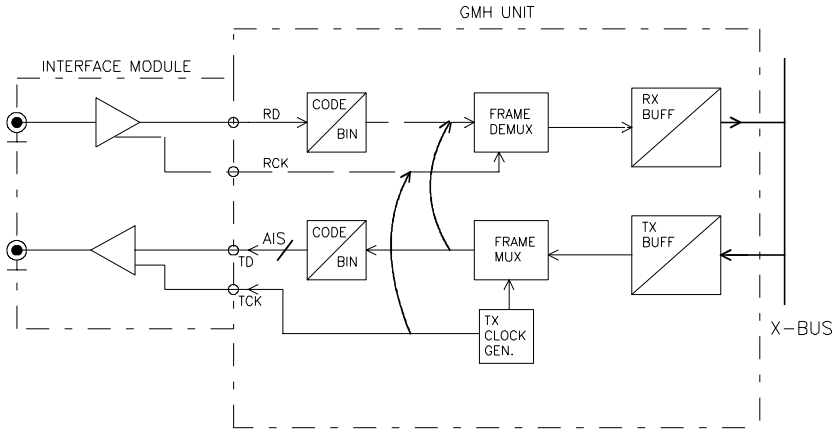


Fig. 4.1-10: Equipment Loop

Line Loop

In the line loop the Rx data received by the interface module is looped back to the interface transmitter. The received clock signal is used as the transmitter clock. AIS is connected to the X-bus instead of the received signal. The yellow alarm LED is switched on.

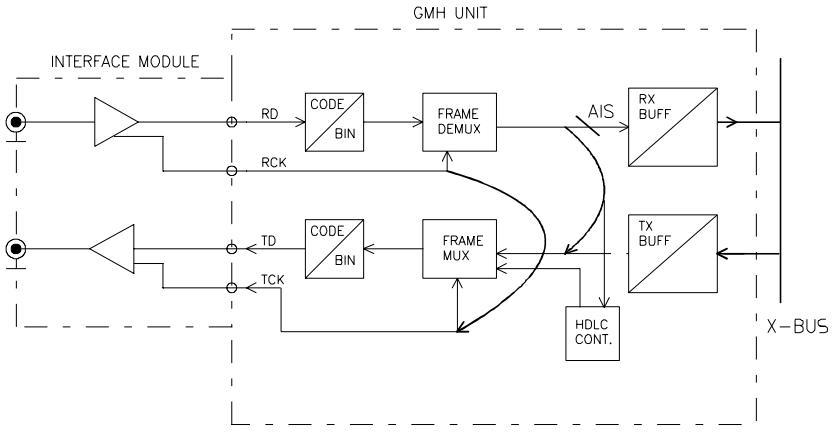


Fig. 4.1-11: Line Loop

The interface module, line coder and decoder as well as the frame demultiplexer and multiplexer can be tested from the module's line connector with the Line Loop Test. When it is used, the HDLC controller works with the line loop. All other bits are looped back to the interface.

Remote Line Loop

The remote line loop operates in the looped unit in the same way as the (local) line loop. The remote line loop is activated from the unit at the other end of the line. The loop is made via the HDLC channel and the control channel continues to operate even when the remote line loop is active. The status of the looped unit can be checked with the service computer. When the loop is made, the yellow LED of the unit which controls the loop is switched on, and the yellow LED of the looped unit is also switched on. The whole line can be tested with the remote line loop.

4.2 INTERFACE MODULES

4.2.1 G703-75 Interface Module

The function of the G703-75 module is to convert signals received by the GMH base unit in a DXX node so that they comply with *G.703* 2048kbit/s asymmetrical 75 ohm specifications and other relevant recommendations concerning electrical interface towards equipment outside the DXX network. The G703-75 module also converts signals from other equipment into signals acceptable to the DXX network.

Module Structure

The G703-75 module consists of three practically independent blocks, i.e. **control block**, **line interface**, and transmitter **phaselock**. The operation of the G703-75 module is controlled via an address bus by a control processor located on the GMH base unit PC board. The block diagram of the G703-75 module is shown below in Fig. 4.2-1.

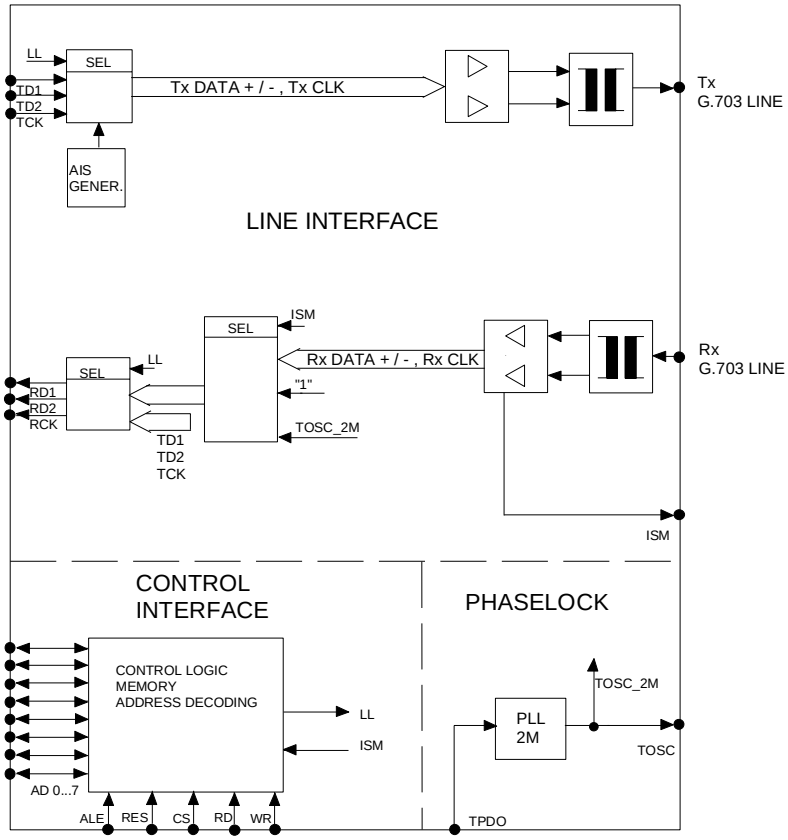


Fig. 4.2-1: G703-75 Block Diagram

Control Block

LL and ISM signals are used in the control block of the unit which handles the communication between the G703-75 and the base unit. The control block also contains address decoding for module registers, a D/A converter and a memory.

Local Loop (LL)
If local loop is commanded from the base unit, the interface module operates as follows: the module produces an AIS alarm indication signal from the TCK signal received from the base unit. The AIS signal is fed to the line transceiver IC and further to the line. Correspondingly the TD1, TD2 and TCK module interface signals are connected back to the base unit interface. This loop is performed on the digital level.

Received Line Signal Missing (ISM)
The G703-75 receiver supervises the input signal level; if this level drops below a threshold, the alarm ISM is activated. Information about this fault is transferred to the base unit via an interface processor bus and also as a direct alarm signal on a dedicated pin of the interface connector. The ISM signal level 1 means that level alarm is activated; moreover, the active ISM causes the incoming data to be replaced by continuous 1, and the incoming clock to be replaced by a transmitter oscillator. Continuous 1 level of data pulses is recognized as AIS signal during retiming in the GMH unit.

Phaselock
The phaselock block comprises of a 2048 kHz voltage controlled transmit oscillator VCO and a PLL filter. Frequency dividers and the phase detector are located in the GMH unit. The TPDO signal supplied by the phase detector is a control signal for the VCO. The oscillator free running frequency is tuned by a D/A converter in case phase locking is lost. This can happen e.g when an SXU unit is removed from the rack.

Line Interface
Because the line interface provided by this module fully complies with all relevant recommendations, a complete specification of this interface is given under Technical Specifications only. The following briefly describes the line interface circuit design of the G703-75 module.

In the **transmit direction** the CMOS level HI-active + pulses and - pulses are inverted and fed to the line transceiver which produces pulse shape according to *G.703* recommendation together with the line transformer and resistors. Output impedance matching to the line is also accomplished with the transformer and resistors. Diode limiters protect against overvoltage.

In the **Receive direction** the line transceiver regenerates CMOS level RD1, RD2 and RCK for the base unit.
The input transformer together with resistors match the line impedance and amplitude for the line transceiver circuit. Diode limiters protect against overvoltage.

Line connectors are 75 Ω SMB type. Front view of the G703-75 is presented in chapter 6.

4.2.2 G703-120 Interface Module

The function of the G703-120 module is to convert signals received by the GMH base unit in a DXX node so that they comply with *G.703* 2048kbit/s symmetrical 120 ohm specifications and other relevant recommendations concerning electrical interface towards equipment outside the DXX network. The G703-120 module also converts signals from other equipment into signals acceptable to the DXX network.

Module Structure

The G703-120 module consists of three practically independent blocks, i.e. **control block**, **line interface**, and transmitter **phaselock**. The operation of the G703-120 module is controlled via an address bus by a control processor located on the GMH base unit PC board. The block diagram of the G703-120 module is shown in Fig. 4.2-2.

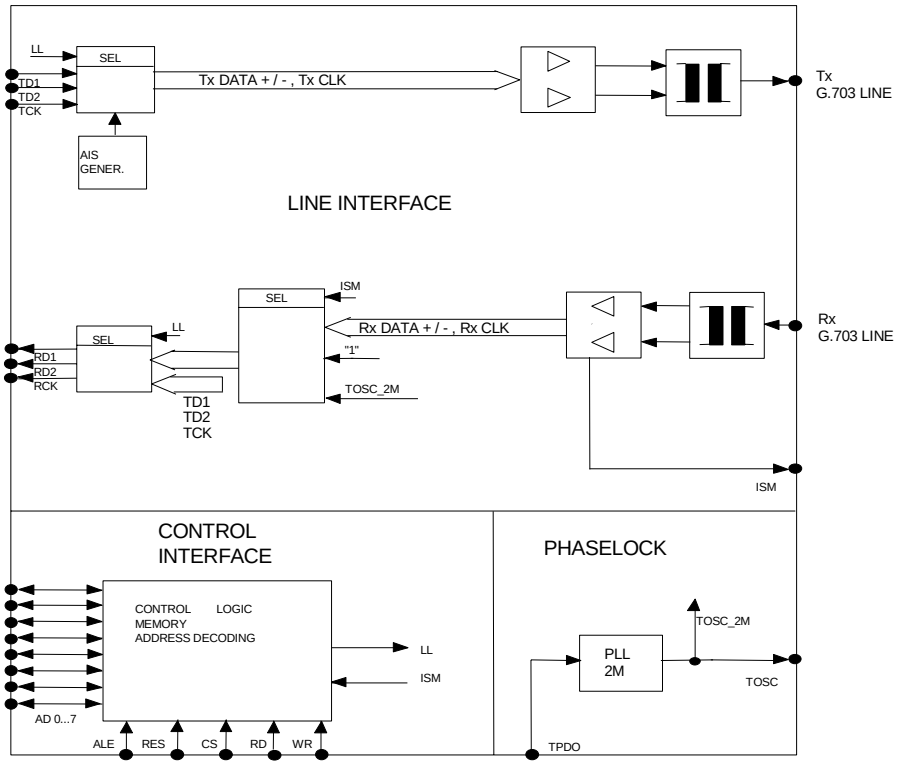


Fig. 4.2-2: G703-120 Block Diagram

Control Block

LL and ISM signals are used in the control block of the unit which handles the communication between the G703-120 and the base unit. The control block contains also address decoding for module registers, a D/A converter and a memory.

Local Loop (LL)

If local loop is commanded from the base unit, the interface module operates as follows: the module produces an AIS alarm indication signal from the TCK signal received from the base unit. The AIS signal is fed to the line transceiver IC and further to the line. Correspondingly the TD1, TD2 and TCK module interface signals are connected back to the base unit interface. This loop is performed on the digital level.

Received Line Signal Missing (ISM)
The G703-120 receiver supervises the input signal level; if this level drops below a threshold, the alarm ISM is activated. Information about this fault is transferred to the base unit via an interface processor bus and also as a direct alarm signal on a dedicated pin of the interface connector. The ISM signal level 1 means that level alarm is activated; moreover, the active ISM causes the incoming data to be replaced by continuous 1, and the incoming clock to be replaced by a transmitter oscillator. Continuous 1 level of data pulses is recognized as AIS signal during retiming in the GMH unit.

Phaselock
The phaselock block comprises of a 2048 kHz voltage controlled transmit oscillator VCO and a PLL filter. Frequency dividers and the phase detector are located in the GMH unit. The TPDO signal supplied by the phase detector is a control signal for the VCO. Oscillator free running frequency is tuned by D/A converter in the case of phase locking is lost. This can happen e.g when SXU unit is removed from the rack.

Line Interface
Because the line interface provided by this module fully complies with all relevant recommendations, a complete specification of this interface is given under *Technical Specification* only. The following briefly describes the line interface circuit design of the G703-120 module.

In the **transmit direction** the CMOS level HI-active + pulses and - pulses are inverted and fed to the line transceiver which produces pulse shape according to *G.703* recommendation together with the line transformer and resistors. Output impedance matching to the line is also accomplished with the transformer and resistors. Diode limiters protect against overvoltage.

In the **Receive direction** the line transceiver regenerates CMOS level RD1, RD2 and RCK for the base unit.
The input transformer together with resistors match the line impedance and amplitude for the line transceiver circuit. Diode limiters protect against overvoltage.

Line connectors are of D-9 type. Front view of the G703-120 is presented in chapter 6.

4.2.3 G703-8M Interface Module

The function of the G703-8M module is to convert signals received by the GMH base unit in a DXX node so that they comply with *G.703* 8448kbit/s asymmetrical 75 ohm specifications and other relevant recommendations concerning electrical interface towards equipment outside the DXX network. The G703-8M module also converts signals from other equipment into signals acceptable to the DXX network.

Module Structure
The G703-8M module consists of three practically independent blocks, i.e. **control block**, **line interface**, and transmitter **phaselock**. The operation of the G703-8M module is controlled via an address bus by a control processor located on the GMH base unit PC board. The block diagram of the G703-8M module is shown below in Fig. 4.2-3.

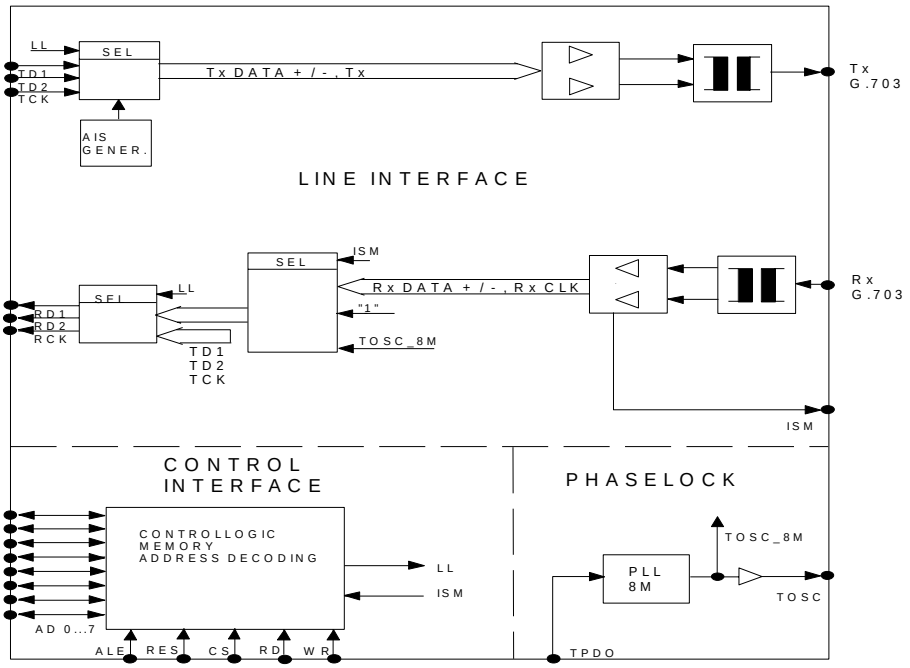


Fig. 4.2-3: G703-8M Block Diagram

Control Block
LL and ISM signals are used in the control block of the unit which handles the communication between the G703-8M and the base unit. The control block also contains address decoding for module registers, a D/A converter and a memory.

Local Loop (LL)
If local loop is commanded from the base unit, the interface module operates as follows:
The module produces an AIS alarm indication signal from the TCK signal received from the base unit. The AIS signal is fed to the line transceiver IC and further to the line. Correspondingly the TD1, TD2 and TCK module interface signals are connected back to the base unit interface. This loop is performed on the digital level.

Received Line Signal Missing (ISM)
The G703-8M receiver supervises the input signal level. If this level drops below a set threshold, the ISM alarm is activated. Information about this fault is transferred to the base unit via an interface processor bus and also as a direct alarm signal on a dedicated pin of the interface connector. The ISM signal level 1 means that level alarm is activated; moreover, the active ISM causes the incoming data to be replaced by continuous 1, and the incoming clock to be replaced by the module PLL oscillator. Continuous 1 -level of data pulses is recognized as AIS signal during retiming in the GMH unit.

Phaselock
The phaselock (PLL) block comprises of a 8448 kHz VCO and a PLL filter. Frequency dividers and the phase detector are located in the GMH unit. The TPDO signal supplied by the GMH phase detector is a control signal for the VCO. The oscillator free running freguency is tuned by a D/A converter.

Line Interface

Because the line interface provided by this module fully complies with all relevant recommendations, a complete specification of this interface is given under *Technical Specifications* only. The following briefly describes the line interface circuit design of the G703-8M module.

In the **transmit direction** the CMOS level HI-active positive and negative transmit pulses are fed to the line transceiver which produces pulse shape according to *G.703* recommendation. Diode limiters protect against overvoltage.

In the **Receive direction** the line transceiver regenerates CMOS level RD1, RD2 and RCK for the base unit.

The input transformer together with related components match the line impedance and signal amplitude for the line transceiver circuit. Diode limiters protect against overvoltage.

Line connectors are of 75 ohm SMB type. Front view of the G703-8M is presented chapter 6.

4.2.4 LTE Interface Module

Structure

The function of the LTE module is to transmit and receive signals between GMH or GCH base units of a DXX and another node of the DXX network, using a symmetrical pair as the transmission medium.

The LTE module consists of three almost independent blocks, i.e. a transmitter, a receiver and the transmitter phaselocks. The operation of the LTE module is controlled by a control processor located on the GMH or GCH base unit PC-board. The block diagram of the LTE module is shown in Fig. 4.2-4.

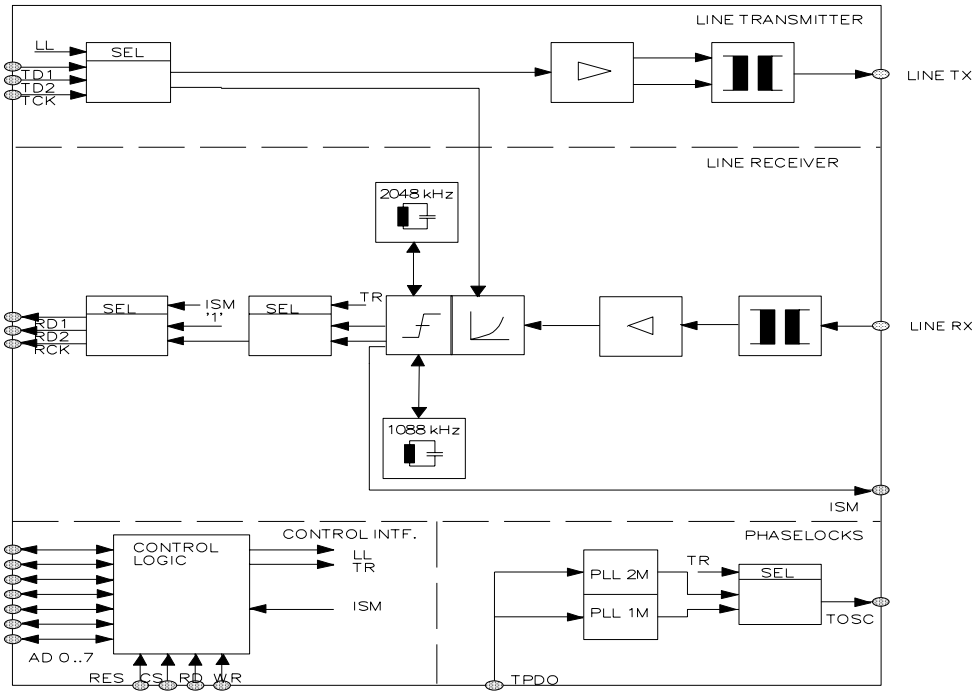


Fig. 4.2-4: LTE Block Diagram

The functions of the LTE module are controlled by the base unit via an address bus. With two control signals, the base unit can change the operational mode of the LTE module. The TR control bit determines the bit rate which is used in the LTE module. The 0-state of the TR bit leads to operation in the 1088 kbit/s mode (= 17/32 x 64 kbit/s), and the 1-state to operation in the 2048 kbit/s mode. The base unit can also command the interface module into a local loop mode, where the outgoing signal is looped back to the interface and an AIS-signal is transmitted to the line. This function is controlled by the LL control bit. The 0-state of the LL bit produces normal operation and the 1-state produces looped operation.

The interface module can also supply information to the base unit whether the line signal is present or not. This is indicated by the ISM alarm bit. 1-state of the ISM means that received line signal input level is not high enough for normal operation. Correspondingly the 0-state of the ISM means that the signal input level is within a suitable range for normal operation. These control signals are used in the **control block** of the unit which handles the communication between the LTE and the base unit.

With the TR-signal the G703 module selects the correct operating rate for the **phase lock block.** This block contains two transmitter phaselocks for the base unit. Both phase locked VCO:s operate continuously, but only the selected clock signal is transmitted to the base unit as the TOSC signal. The phaselocks receive the control signal TPDO from the base unit.

Line transmitter block performs an adaptation of the data pulses to the line. The transmitter operates independently of the actual bit rate, but if local loop is selected then the transmitter block generates a suitable AIS signal from the incoming clock TCK and transmits this AIS signal to the line when TD1 and TD2 data signals are looped back to the base unit.

Line receiver block receives distorted and attenuated data pulses from the symmetrical line and regenerates a suitable clock for the receiver timing performed in the base unit. The received data pulses are first buffered and the distortion caused by the line is equalised after which the pulses are fed to the regenerator IC where the data is regenerated and the clock recovered with a tank circuit.

The interface signal input level is also supervised and the alarm signal ISM is generated if the input level exceeds preset limits. The bit rate is selected according to the state of TR bit. Finally the received data and clock signals are fed to the base unit.

Local Loop

If local loop is commanded from the base unit the interface module operates as follows: The module produces an AIS-signal from the TCK clock signal received from the base unit. This AIS-signal is fed to the transmitter selector and normally not used for any other purpose, but when the loop is activated the selector selects the AIS to be connected to the line and correspondingly the TD1, TD2 and TCK interface signals to be connected back to the base unit interface. This loop is performed on the analogue level just after the line receiver input buffer.

Received Line Signal Missing

The line receiver supervises the input signal level and if this level drops below a selected threshold, the alarm ISM is activated. Information about this fault is transferred to the base unit via the interface processor bus and also as a direct alarm signal on a dedicated pin of the interface connector. The ISM signal level 1 means that level alarm is activated, and the active ISM causes moreover the incoming data to be replaced by continuous 1 and the incoming clock to be replaced by the transmitter clock TPDO. Continuous 1-level of data pulses is recognised as AIS signal during retiming.

Line Interface

A complete specification of this interface module is presented in the technical specification only. The following describes briefly the design of interface circuits of the LTE module.

In the transmit direction the transmitted **+** pulses and **-** pulses are fed separately to the module pulse amplifier. CMOS level LO-active pulses drive bipolar pulse current amplifiers which drive a centre tapped double wound transformer to produce secondary output pulses that are ternary according to the HDB3 coding rule. Because the LTE module uses a standardised and well known line code like HDB3 the further explanation of the line code is omitted here; it can be found in the relevant ITU-T[1] recommendations. Receive direction cable shield can be grounded with S2 and transmit direction with S1 respectively. The connector type of this interface module is D-9 (symmetrical 120 Ohm).

The line receiver includes input frequency band limitation immediately after the input transformer, followed by diode limiters. A buffer amplifier provides an effective decoupling of the input transformer from the receiver electronics in order to obtain a favourable pure resistive return loss to the interface.

The detection of weak incoming data signals is performed by a linear automatic line build out circuit (ALBO) which contains all essential functions for complete regeneration of the data. Only the frequency response and line equalisation parameters are optimised for the used bit rates 2048 and 1088 kbit/s. The detection IC also regenerates the clock from the received data using proper tank circuits but the retiming of the data is performed later on the base unit. Regenerated data and clock signals are fed to a receive direction selector. The performance of the line receiver depends essentially on two parameters. When the bit rate is 2048 kbit/s the most important parameter is the line attenuation. When the used bit rate is 1088 kbit/s, also crosstalk may limit the maximum achievable transmission distance. If the operator desires line lengths approaching 3 km, the crosstalk should be minimised.

A front view showing the connection of signals in the line interface is shown in chapter 6.

4.2.5 OTE Interface Module

Structure

The function of the OTE module is to convert signals received by GMH or GCH base units of a EricssonDXX node into a suitable format for transmission via optical fiber to the remote end of a connection in the EricssonDXX network. In the receiving direction the OTE module regenerates signals and transfers them without bit errors to a base unit. The OTE module can be furnished with an optical LED transmitter or a standard LASER transmitter, the choice depending mainly on the required transmission distance.

The OTE module consists of three almost independent blocks, i.e. a transmitter, a receiver and the transmitter phase locks. The operation of the GDH module is controlled by a control processor located on the GMH or GCH base unit PC board.

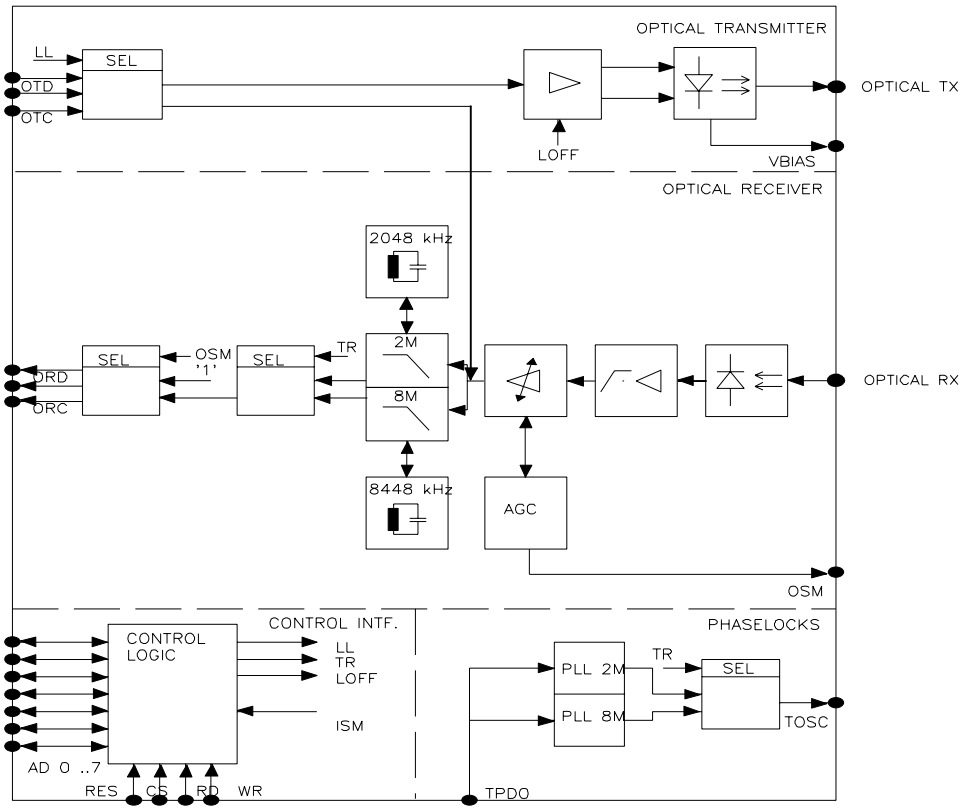


Fig. 4.2-5: OTE Block Diagram

Local Loop

If local loop is commanded from the base unit the interface module operates as follows: The module produces an AIS-signal from the OTC clock signal received from the base unit. This AIS signal is fed to the transmitter selector and normally not used for any other purpose, but when the loop is activated the selector selects the AIS to be connected to the line and correspondingly the OTC interface signal to be connected back to the base unit interface. This loop is performed immediately after the main AGC amplifier.

Received Line Signal Missing

The optical receiver supervises the input signal level and if this level drops below a selected threshold, the alarm OSM is activated. Information about this fault is transferred to the base unit via the interface processor bus and also as a direct alarm signal on a dedicated pin of the interface connector. The OSM signal level 1 means that level alarm is activated, and the active OSM causes moreover the incoming data to be replaced by continuous 1 and the incoming clock to be replaced by the transmitter clock TPDO. Continuous 1-level of data pulses is recognized as AIS signal during retiming.

LOFF

When a LASER transmitter is used it is possible to switch off the optical transmitter automatically, if a break occurs in the optical cable. If a cable break occurs when the automatic transmitter switch off is activated, the first optical receiver on the connection detects the loss of the optical signal and will switch off its own transmitter. After that the receiver in the other end will also detect the loss of the optical signal and correspondingly switch off its own transmitter. This means that if only one of the fibres is broken, also then it is possible to switch off the connection. Normally this kind of operation is not used, because when the fault has been removed the LASERs will not be switched on automatically, and the switch on must be forced manually at either one of the transmitters.

Optical Interfaces

The OTE modules use standard CMI code as the line code. The CMI code is preferred because there is a very good balance between ones and zeroes, a clear spectral component on the clock frequency, and it also presents simple methods for coding and decoding. On the other hand CMI doubles the bandwidth needed for transmission. This presents no problem concerning the fiber, but the noise bandwidth is increased in the receiver which leads to some loss of sensitivity. The coding table of the CMI code is shown in the table below, where it is shown that it is possible to use the received symbol **10** for error detection purposes.

Transmitted Data Bit	CMI Coded Line Symbol
0	01
1	00 or 11, alternating

The **optical transmitter block** performs an adaptation of data pulses to the line. The transmitter operates independently of the used bit rate, but when local loop is selected then the transmitter block generates a suitable AIS signal from the incoming clock TCK and transmits this AIS signal to the line while OTD data signal is looped back to the base unit. The LED transmitter is a simple current switch passing the modulating current through the LED when the transmitted symbol is one, and cutting off the current when the transmitted symbol is zero. A laser transmitter is more complicated because the threshold current of a semiconductor LASER strongly depends on the temperature. Therefore a LASER unit also includes an optical PIN diode detector, whose function is to detect the output power of the LASER and to generate a control signal to the control circuit continuously regulating the bias current. If the temperature increases, the threshold current of the LASER also increases, which leads to a decreased optical output power; in order to compensate this the bias current through the LASER is increased. The modulation of the LASER is designed so that the laser component is biased with a mean bias current c. 20 mA above the threshold current; the modulation for symbol zero is obtained by decreasing the current very close to the threshold, and correspondingly the modulation for symbol one is obtained by increasing the bias current about 20 mA above the bias mean value.

The optical receiver block consists of several functions which are required for operation with both 2 Mbit/s and 8 Mbit/s. The received optical power is first converted to an electrical current in the PIN diode detector followed by a high impedance FET preamplifier in order to guarantee maximum sensitivity of the receiver. A high impedance design usually causes an unwanted bandwidth limitation which is equalized in the equalizing amplifier. Adaptation for different line lengths is achieved by adjusting the gain of the AGC amplifier. The amplified data signal is fed to the 2 and 8 MHz filters and digitizing circuits. The selection of the used bit rate is made on the digital level so that it will not interfere with the analogue part of the receiver. The optical signal input level is also supervised, and an alarm signal OSM is generated if the level falls below a selected value. The state of the TR bit controls the bit rate selection. Finally the received data and clock signals are fed to the base unit.

A standard optical connector of FC-type with receptacle is used in the OTE modules. The interfaces are shown in chapter 6.

4.2.6 HDSL interface module

Applications

The HCE-2M-2P and HCE-2M-1P HDSL modules are designed for connecting the HDSL modems (NTUs) HTU-2M and OTU-2M to DXX networks together with the GMH unit. The modules can also be used without the NTU as a trunk interface.
All modules are designed for HDSL transmission over physical 1- or 2-pair copper wires using the 2B1Q line code. Transmit and receive directions use the same pairs. Depending on the rate and the cable type used, these HCE modules can support cables that are up to 3-10 km long.
HCE-2M-2P meets ETS 101 135 (HDSL) in 2-pair mode (1168 kbit/s / pair).
The proprietary line rate of 595 kbit/s is also included.
HCE-2M-1P meets ETS 101 135 in 1-pair mode (2320 kbit/s).
The proprietary line rates of 1168 and 592 kbit/s are also included.

Structure

HCE-2M-2P and HCE-2M-1P use the same ASICs and uP but they have different AFE (Analog Front End). The front panel of the HCE module is shown in Fig. 4.2.

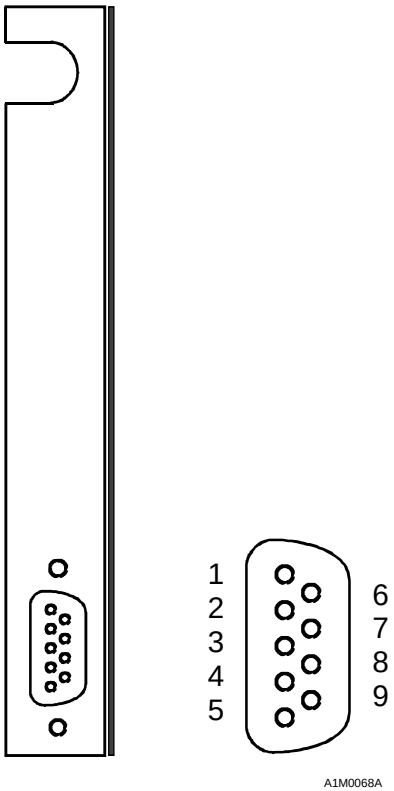


Fig. 4.2-6 HCE Front Panel

Pin	HCE-2M-2P	HCE-2M-1P
1 and 2	pair 2	pair 1
4 and 5	pair 1	
6 and 7	pair 2 RPF in	pair 1 RPF in
8 and 9	pair 1 RPF in	

RPF is Remote Power Feed for OTU.

Functional Structure

All the transmission functions of HCE-2M have been implemented by an ASIC.

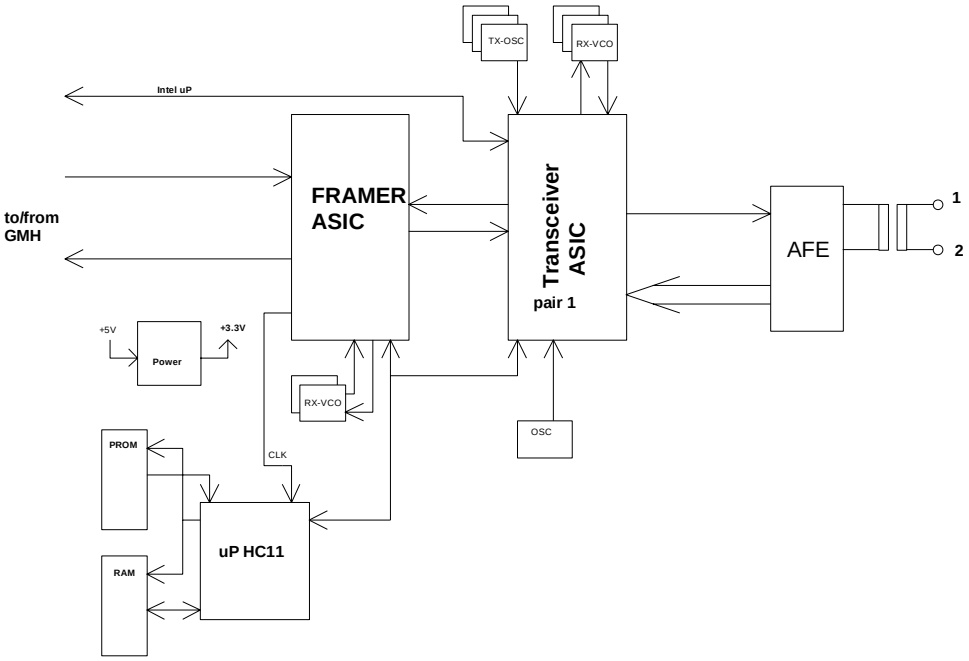


Fig. 4.2-7: HCE-2M-1P Block Diagram

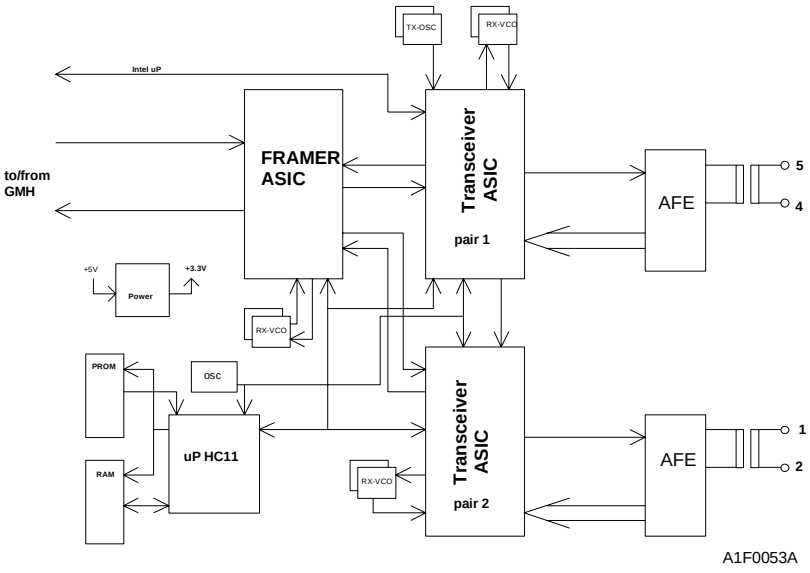


Fig. 4.2-8 HCE-2M-2P Block Diagram

All the configurable parameters of the HCE modules are controlled by the main unit (GMH) software.

Operation

Line Transmission
The transmit data is fed to a scrambler which makes the transmit spectrum independent from the transmitted data pattern. The scrambled data signal is then fed to a 2B1Q coder, which maps two bits in on transmitted 4-level signal. This 4-level digital signal is then converted to analog and filtered with a transmit filter.
On the receiver side the data is first filtered to remove unnecessary frequency components and to limit received signal bandwith suitable for receiver signal processing. An automatic signal level adjustment is implemented together with the receiver filter. The level adjustment is controlled by the uP. The analogue line signal at the constant level is converted to a sampled digital signal by an A/D converter. This signal, which is distorted by the line attenuation, is fed to the ASIC where Echo cancelling and adaptive equalisation algorithms are calculated to equalise the impairments caused by the line and own transmitted signal.
The received clock is derived from the line signal and the optimum sampling clock is fed to the A/D converter. The optimum sampling phase is maintained by a receiver PLL, controlled by ASIC.
After equalisations and transmitted symbol decoding the transmitted bits are extracted from the symbol and the bits are fed to the descrambler. The descrambled data is fed to the main unit.
The received line signal level is calculated by a uP. The received signal noise margin is estimated by calculating the received signal to noise ratio after line equalising. This is also done in a uP.

Test Loops

Interface Loop

The Interface Loop is shown in
Fig. 4.2-9.

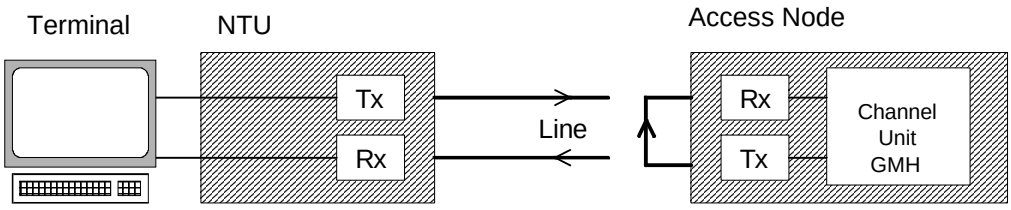


Fig. 4.2-9: Interface Loop

During the line loop the transmitted line signal is looped back to the receiver before the line transformer.

5 SUPERVISED FAULT CONDITIONS

Terminology:

Maintenance Status:

PMA	=	Prompt Maintenance Alarm
DMA	=	Deferred Maintenance Alarm
MEI	=	Maintenance Event Information

Service Status:

S	=	Service Alarm

LED Indications:

R	=	Red alarm LED
Y	=	Yellow alarm LED
RB	=	Red alarm LED blink

Consequent Actions:

TxAIS	=	AIS insertion to Tx signal
RxAIS	=	AIS insertion to Rx signal
TxTS-AIS	=	AIS insertion in time slots of Tx signal
FrFEA	=	Frame level far-end alarm (ts0/B3 in 2Mbit/s frame, ta66/B7 in 8 Mbit/s frame)
MFrFEA	=	Multiframe level far-end alarm (FR0/ta sig/B6)

MFrFEA is also transmitted if FrFEA is transmitted.

5.1. FAULTS COMMON PART (BASIC CONFIGURATION)

Common logic faults

Fault Condition	**Status**	**LED**	**Note**
Reset of Unit	PMA	Red	(1)
Power Supply Faults	**Status**	**LED**	**Note**
Power + 5 V	PMA	Red	
Power + 12 V	PMA	Red	
Power - 10 V	PMA	Red	
Memory Faults	**Status**	**LED**	**Note**
RAM Fault	PMA	Red	
EPROM Fault	PMA	Red	
Flash Write Error	PMA	Red	
Flash Copy Error	PMA	Red	
Flash Erase Error	PMA	Red	
Flash Duplicate Error	PMA	Red	
Flash Shadow Error	PMA	Red	
Flash Check Sum Error	PMA	Red	
Missing Settings	PMA	Red	
Incompatible SW in EPROM and FLASH	PMA	Red	
Cross-Connection Faults	**Status**	**LED**	**Note**
X-Connect RAM Fault	PMA	Red	
Block 1/2/3/4 IA Fault	PMA	Yellow	
Loss of Master Clock Locking	MEI	-	
Fallback list Warning	MEI	-	
Loss of External Clock	PMA	Red	
Phase Locked Loop Alarm	PMA	Red	
External Clock Warning	MEI	-	
Clock Far End Alarm of Choice 1/2/3/4/5	MEI	Yellow	
Flash List Check Sum Error	PMA	Red	
ASIC Latch Error	PMA	Red	
ASIC Latch Warning	MEI	-	
Time Controlled X-connect Warning	PMA	-	
X-Connect Flash List Conflict	MEI	-	
PortDesc Flash List Conflict	MEI	-	
Swapped Trunk Flash List Conflict	MEI	-	
Passivated Trunk Flash List Conflict	MEI	-	
Unit IA Fault	PMA	Yellow	
Inventory Faults	-	-	
Missing Unit	PMA	Yellow	
Extra Unit	MEI	Yellow	

(1) Fault message (with delta event) appears when the unit starts to operate.

Rx signal faults

Signal & Frame Faults	**Status**	**LED**	**Rx signal**	**Tx signal**
Interface module missing	PMA, S	R	RxAIS	-
Wrong interface module	PMA, S	R	RxAIS	Tx signal cut
Rx signal missing	PMA, S	R	RxAIS	FrFEA
Rx signal is AIS	MEI, S	Y	RxAIS	FrFEA
Loss of frame alignment 1 Frame alignment lost 2 Frame alignment lost by CRC -> 915/1000 errored CRC-blocks 3 CRC missing	 PMA, S PMA, S DMA	 R R R	 RxAIS RxAIS RxAIS	 FrFEA FrFEA FrFEA
BER 10^{-3} - frame alignment word (normal error response) - line code errors - n x 64 kbit/s baseband signal	PMA, S	R	RxAIS	FrFEA
Wrong input signal 1 Own NNM messages received 2 Wrong IDs in NNM messages (detection can be inhibited) 3 No response to NNM message	 PMA, S PMA, S PMA, S	 R R R	 RxAIS RxAIS RxAIS	 - - -
Loops	**Status**	**LED**	**Rx signal**	**Tx signal**
Local loops 1 Interface back to equipment 2 MUX/DEMUX back to eq. 3 MUX/DEMUX back to line 4 Line loop made by neighbour	 MEI, S MEI, S MEI, S MEI, S	 Y Y Y Y	 - - RxAIS RxAIS	 TxAIS TxAIS - -
Remote loops Remote controlled line loop	 MEI, S	 Y	 -	 -
Multi frame level faults	**Status**	**LED**	**Rx signal**	**Tx signal**
Multiframe alignment lost (group N)	PMA, S	R	RxAIS/ SigTS	MFrFEA
AIS in signalling (group N)	MEI, S	Y	RxAIS/ SigTS	MFrFEA
Far end alarms	**Status**	**LED**	**Rx signal**	**Tx signal**
Frame far-end alarm (FrFEA)	MEI, S	Y	RxAIS/ SigTS	RxAIS operation can be turned off
Multiframe far-end alarm (MFrFEA)	MEI, S	Y	RxAIS/ SigTS	RxAIS operation can be turned off
Degraded signal	**Status**	**LED**	**Rx signal**	**Tx signal**
Error rate 10^{-3} - frame alignment word (AIS insertion inhibited)	DMA	R	-	-
Error rate 10^{-6} - CRC block errors - line code errors (used for speeds over 1 Mbit/s)	DMA	R	-	-
Frequency difference - excessive phase drift in input buffer	DMA	R	-	-
Buffer slips/1 hour	MEI	RB	-	-

5.2 OPTIONAL INTERFACE UNIT (GMH)

Tx Signal Faults (Block 1, 2)

Fault Condition	**Status**	**LED**	**Tx signal**
Tx Clock fault (PLL)	PMA, S	R	TxAIS
Bus faults IA activity missing Bus sync. fault (block 0)	 PMA, S PMA, S	 R Y	 TxTS-AIS TxTS-AIS
AIS from X-bus	MEI, S	Y	TxAIS (1)
BTE Tx line test	MEI, S	Y	Test pattern

(1) Only when FAS is transferred through the network

Rx Signal Faults (Block 1,2)

Signal & Frame Faults	**Status**	**LED**	**Rx signal**	**Tx signal**
Interface module missing	PMA, S	R	RxAIS	-
Wrong interface module	PMA, S	R	RxAIS	Tx signal cut
Rx signal missing	PMA, S	R	RxAIS	FrFEA
Rx signal is AIS	MEI, S	Y	RxAIS	FrFEA
Loss of frame alignment Frame alignment lost Frame alignment lost by CRC -> 915/1000 errored CRC-blocks CRC missing	 PMA, S PMA, S DMA	 R R R	 RxAIS RxAIS RxAIS	 FrFEA FrFEA FrFEA
BER 10^{-3} - frame alignment word (normal error response) - line code errors - n x 64 kbit/s baseband signal	PMA, S	R	RxAIS	FrFEA
Wrong input signal Own NNM messages received Wrong IDs in NNM messages (detection can be inhibited) No response to NNM message	 PMA, S PMA, S PMA, S	 R R R	 RxAIS RxAIS RxAIS	 - - -
NTU problems NTU power off/local loop NTU line break NTU short circuit	MEI MEI MEI MEI	Y Y Y Y	- RxAIS - -	- - - -
ASIC register error	PMA, S	R	-	-
Loops	**Status**	**LED**	**Rx signal**	**Tx Signal**
Local loops Interface back to equipment MUX/DEMUX back to eq. MUX/DEMUX back to line Line loop made by neighbour	 MEI, S MEI, S MEI, S MEI, S	 Y Y Y Y	 - - RxAIS RxAIS	 TxAIS TxAIS - -
Remote loops Remote controlled line loop	 MEI, S	 Y	 -	 -

Multiframe level faults	**Status**	**LED**	**Rx signal**	**Tx signal**
Multiframe alignment lost (group N)	PMA, S	R	RxAIS/ SigTS	MFrFEA
AIS in signalling (group N)	MEI, S	Y	RxAIS/ SigTS	MFrFEA
Multiframe faults of the 8 Mbit/s signal are detected separately in each of the four signalling time slots (groups).				
Far-end alarms	**Status**	**LED**	**Rx signal**	**Note**
Frame far-end alarm (FrFEA)	MEI, S	Y	RxAIS/ SigTS	RxAIS operation can be turned off
Multiframe far-end alarm (MFrFEA)	MEI, S	Y	RxAIS/ SigTS	RxAIS operation can be turned off
Degraded signal	**Status**	**LED**	**RxAIS**	**FrFEA**
Error rate 10^{-3} - frame alignment word (AIS insertion inhibited)	DMA	R	-	-
Error rate 10^{-6} - CRC block errors - line code errors (used for speeds over 1 Mbit/s)	DMA	R	-	-
Frequency difference - excessive phase drift in input buffer	DMA	R	-	-
5.4 Buffer slips/1 hour	MEI	RB	-	-

Miscellaneous Faults (Block 1, 2)

Fault Condition	Status	LED	Rx signal	Tx signal
Port locking conflict	DMA	R	-	-
HDLC overlap with X-bus	DMA	R	-	-
Master clock RAI overlap with X-bus	DMA	R	-	-
G821 unavailable state	PMA, S	-	-	-
G821 limit event	DMA	-	-	-
Faults masked/Test	MEI	Y	-	-

1+1 Protection Switch Fault Messages (Block 0)

Fault Condition	**Status**	**LED**	**Rx signal**	**Tx signal**
Protection switch forced	MEI	R	-	-
Loss of protected signal	PMA, S	R	- (1)	- (1)

Common Logic Faults (Block 0)

Fault Condition	Status	LED	Rx signal	Tx signal	Note
Reset	PMA, S	R	Bus if off	Off	(3)
Power supply (5V,+12V,-10V)	PMA	R	-	-	(2)
CPU memory faults RAM fault EPROM fault FLASH faults	PMA, S	R	-	-	-
Incompatible EPROM/FLASH SW	PMA	R	-	-	-
Check sum err in downloaded SW	PMA	R	-	-	-
SW unpredicted	PMA	R	-	-	-
Missing settings	PMA, S	R	-	-	-
Start request denied	PMA, S	R	Bus IF off	AIS	-
Tx RAM error	PMA, S	R	-	-	-
Rx RAM error	PMA, S	R	-	-	-

(1) Signal actions depend on actions of the protected interfaces.
(2) Rx signal action depends on the frame level alarm of the corresponding interface.
(3) Fault message (with delta event) appears when the unit starts to operate.

Miscellaneous Faults

Fault condition	Status	LED	Rx signal	Tx signal
Port locking conflict	DMA	R	-	-
HDLC overlap with X-bus	DMA	R	-	-
Master clock RAI overlap with X-bus	DMA	R	-	-
G821 unavailable state	PMA, S	-	-	-
G821 limit event	DMA	-	-	-
Faults masked/Test	MEI	Y	-	-

1+1 Protection switch faults

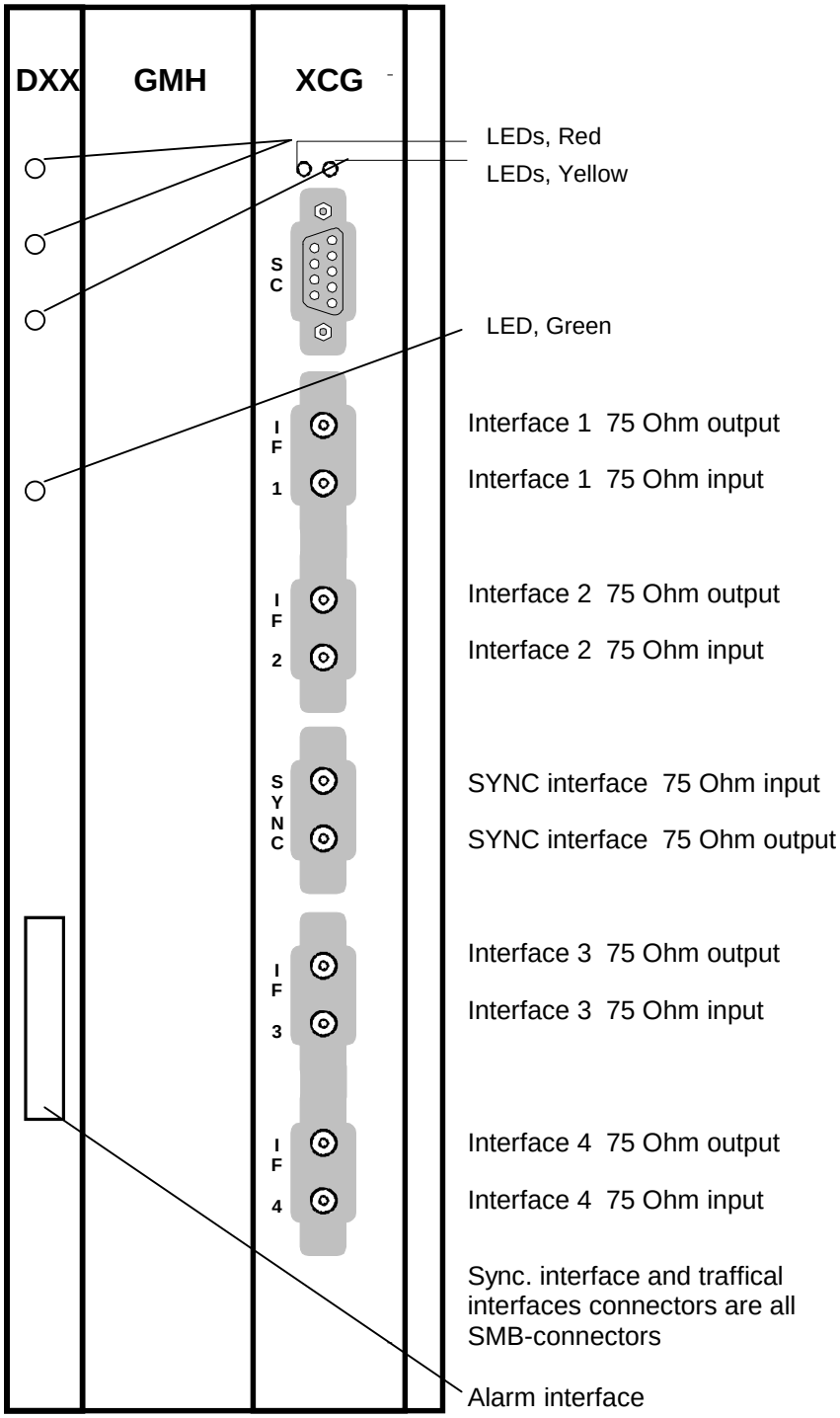
Fault condition	Status	LED	Rx signal	Tx signal
Protection switch forced	MEI	R	-	-
Loss of protected signal	PMA, S	R	- (1)	- (1)

(1) Signal actions depend on actions of the protected interfaces.

6 UNIT CABLING DATA

6.1 UNIT CABLING DATA FOR DXX PLUG-IN UNIT- COMMON PART

6.1.1 PLUG-IN UNIT WITH 75 OHM



SC Connector Pin Assignment

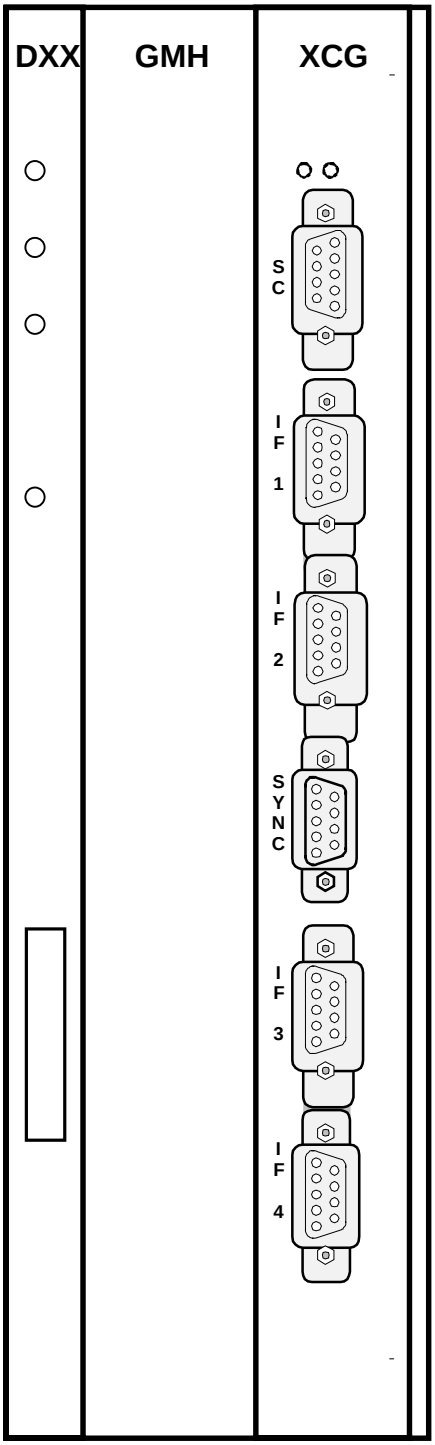
D-type 9 pin female connector

Pin	CCITT V.24 Circuit Number	In/Out	Signal
1	109	out	Signal detector
2	104	out	Received data
3	103	in	Transmitted data
4	108	in	Data terminal ready
5	102	-	Signal ground
6	107	out	Data set ready
7	105	in	Request to send
8	106	out	Ready for sending
9	-	-	no connection

Service Computer Connector, 9-pin to 25 pin conversion table

Pin Number at D-9	Pin Number at D-25	CCITT V.24 Circuit Number
1	8	109
2	3	104
3	2	103
4	20	108
5	7	102
6	6	107
7	4	105
8	5	106
9	-	-

6.1.2 PLUG-IN UNIT WITH 120 OHM



SC Connector Pin Assignment

Pin	CCITT V.24 Circuit Number	In/Out	Signal
1	109	out	Signal detector
2	104	out	Received data
3	103	in	Transmitted data
4	108	in	Data terminal ready
5	102	-	Signal ground
6	107	out	Data set ready
7	105	in	Request to send
8	106	out	Ready for sending
9	-	-	no connection

SYNC Interface Connector

Pin	Signal
1	120 Ohm input
2	120 Ohm input
3	GND
4	120 Ohm output
5	120 Ohm output
6	GND
7	GND
8	GND
9	GND

G.703 / 120 Ohm interface connectors 1-4

Pin	Signal
1	120 Ohm output
2	120 Ohm output
3	GND
4	120 Ohm input
5	120 Ohm input
6	GND
7	GND
8	GND
9	GND

All connectors are D-type 9 pin female connectors

6.2 ALARM OUTPUTS

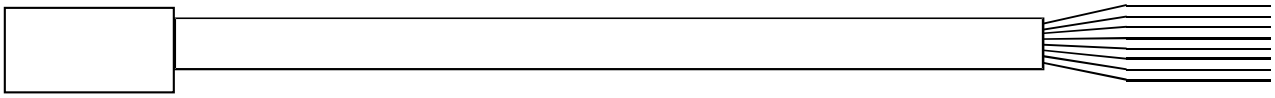
Flat connector at the extension unit

1 - MEI, in to relay
2 - MEI, out (alarm state= loop closed)
3 - MEI, out (alarm state= loop open)
4 - DMA, in to relay
5 - DMA, out (alarm state= loop closed)
6 - DMA, out (alarm state= loop open)
7 - PMA, in to relay
8 - PMA, out (alarm state & power off= loop open) *
9 - PMA, out (alarm state & power off= loop closed) *
10 - GND

** The PMA alarm output is configured that the relay is in active state during alarm free conditions and goes to non active state during alarm or power off.*

Cabling for unit alarm to BTS

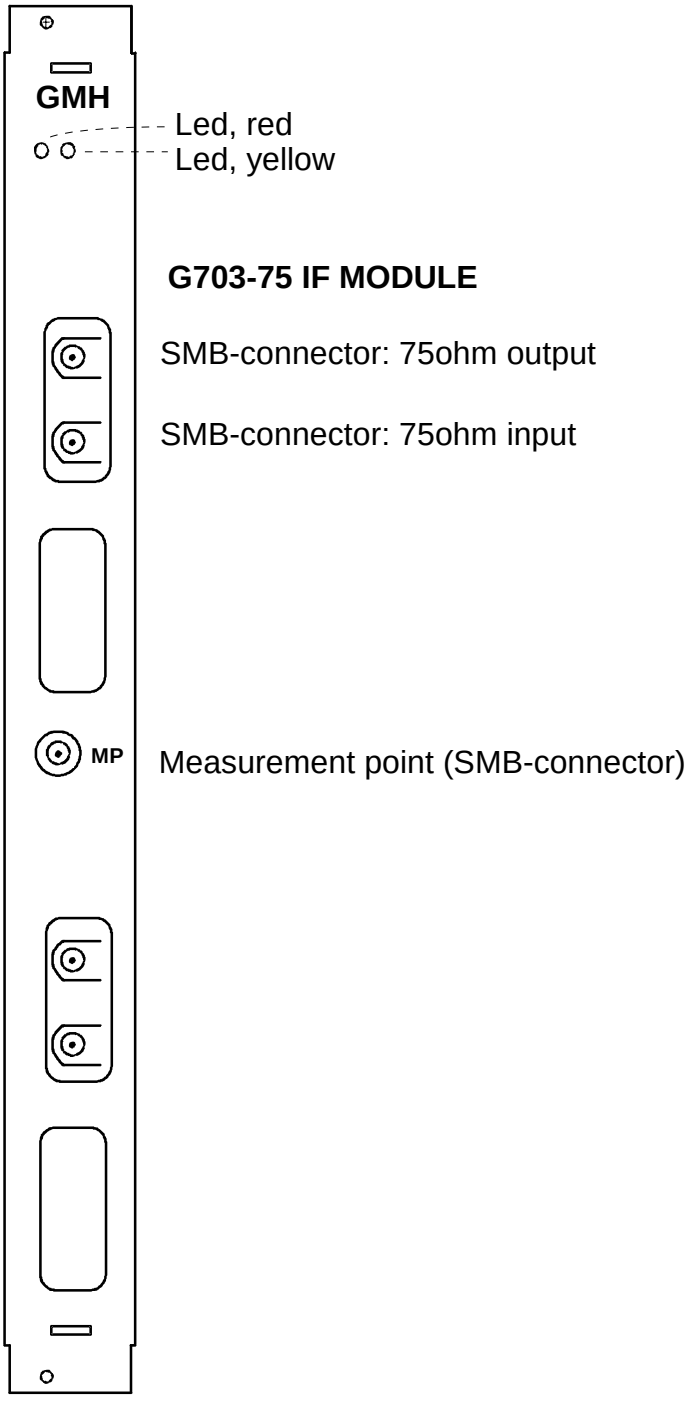
Use twisted pair cable, category 5



6.3 UNIT CABLING DATA FOR OPTIONAL UNIT

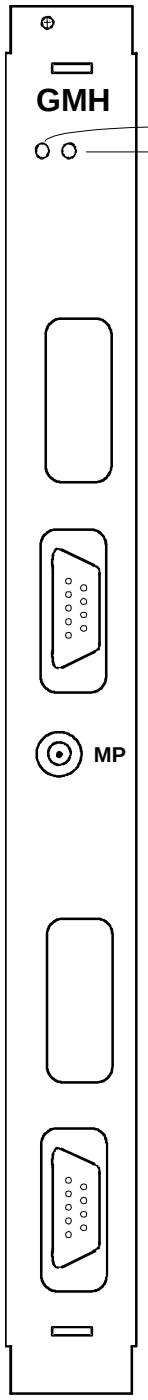
Unit Cabling Data for Interface 75 Ohm 2 and 8 Mbit/s

Front Panel for GMH with G703-75



Unit Cabling Data for 120 Ohm 2 Mbit/s Interface

Front Panel for GMH with G703-120



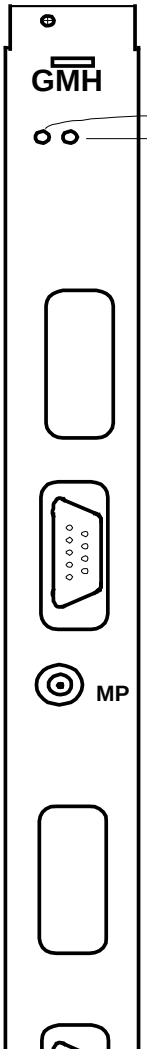
D-type 9 pin female connector

Pin	Signal
1	120 ohm output
2	120 ohm output
4	120 ohm input
5	120 ohm input
6	Tx Cable shield
9	Rx Cable shield

Measurement point (SMB-connector)

Unit Cabling Data for 120 Ohm 2 Mbit/s long-haul Interface

Font panel for GMH with LTE



Led, red
Led, yellow

LTE IF MODULE

D-type 9 pin female connector

Pin	Signal
1	Transmit signal B
2	Transmit signal A
4	Receive signal B
5	Receive signal A
6	Cable shield output
9	Cable shield input

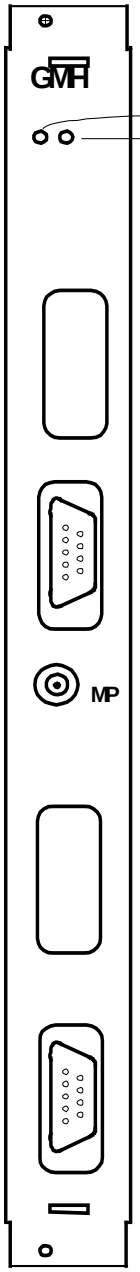
Measurement point (SMB-connector)

Cabling for GMH with LTE

4-wire	2-wire	Pin No	Pair	Color	Remarks
Tx A	-	1	1	blue	
Tx B	-	2	1	blue-white	
Rx A	Rx/Tx A	4	2	orange	
Rx B	Rx/Tx B	5	2	orange-white	
Shield Tx	-	6			
Shield Rx	Shield Rx/Tx	9	Shield	bright	Connect the shield to the connector shell

Unit Cabling Data for 0.5 to 2 Mbit/s HDSL Interface

Font panel for GMH with HCE-1P or HCE-2P



D-type 9 pin female connector

Pin	Signal
1	See table below

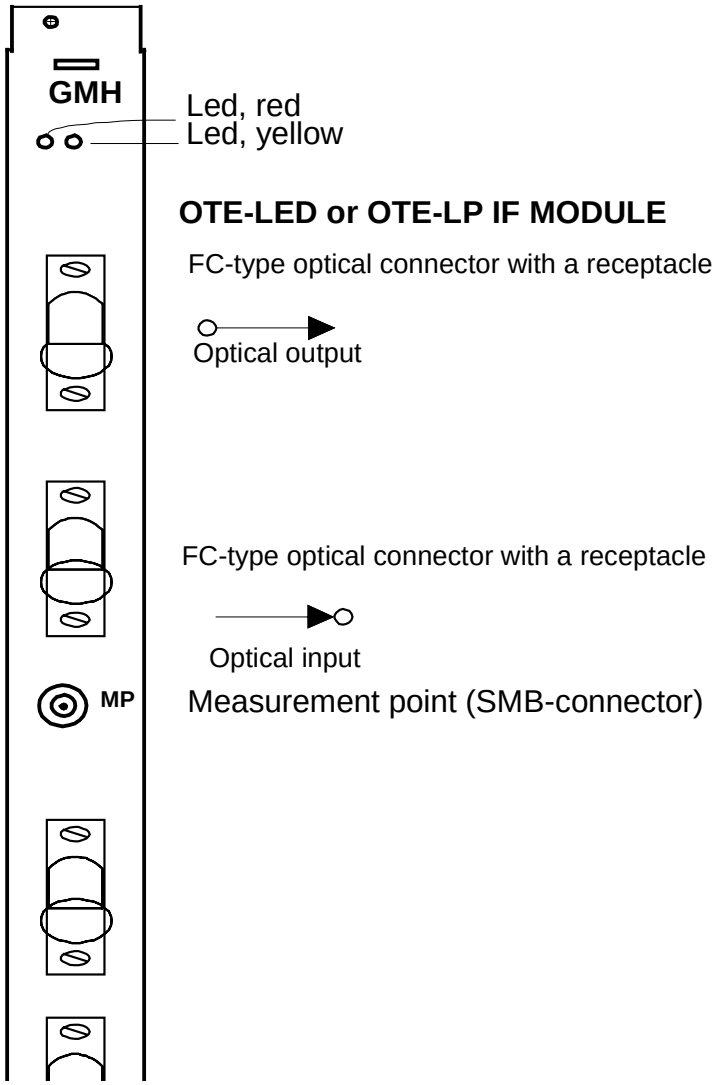
Measurement point (SMB-connector)

Cabling for GMH with HCE interface module

Pin	**2 Pair module**	**1 Pair module**	**Remarks**
1 and 2	Pair 2	Pair 1	
4 and 5	Pair 1	-	
6 and 7	Pair 2 RFP in	Pair 1 RPF in	RPF = Remote power feed for OTU
8 and 9	Pair 1 RPF in	1	RPF = Remote power feed OTU
3			Not used

Unit Cabling Data for Optical 2 and 8 Mbit/s Laser or LED Interface

Front Panel GMH with OTE-LED or OTE-LP



7 TECHNICAL SPECIFICATIONS

Cross-Connect

Cross-connection method	Synchronous time slot interleaving
Frame frequency	8 kHz
Capacity: The sum of cross-connected signals	64 Mbit/s
Smallest cross-connect unit	8 kbit/s
Signalling cross-connection (XD)	n x 500 bit/s (CAS)
Delay of cross-connect core:	1 frame = 125 µs 2ms n x 64 kbit/s CAS-bits (500 bit/s)
Time integrity between time slots in cross-connected signals is maintained	
CAS TS capacity	= 32 bus time slots
n x 8 kbit/s cross-connect port capacity	= 95 bus time slots

Timing

Master clock frequency	16 896 kHz +/- 30 ppm
Master clock functional modes	Locking to the IF rx clock (n x 64 kbit/s) n = 1 to 32 Locking to external clock input (n x 64 kHz) Clock fallback list (5 levels + internal mode)
Frame sync.	8 kHz (125 us)
Multiframe sync (E1)	500 Hz (2ms)
Multiframe sync (T1)	166.66 Hz (6 ms)
Locking frequency	n x 64 kHz +/- 50 ppm
External clock input	n x 64 kHz (n = 1 to 32) +/- 50 ppm Electrically G.703 (120 / 75 Ohms)
External clock output	2048 kHz +/- 30 ppm (Locked to master clock) Electrically G.703 (120 / 75 Ohms)
Jitter transfer function and jitter in the output	G.736, G.823

The 16.896 Mhz clock is used to generate the main clock for whole Transport Module (TM).

Control Interface Specifications

Service Computer Interface	
Purpose	Management interface for SC/DXX Manager
Electrical interface	V.28
Data bit rate	9600 b/s asynchronous
Character format	8 bit, no parity, 1 stop bit
Connector type	D-type 9-pin female connector
Interface signals	102,103,104,105,106,107,108 and 109
Protocol	Layers 2…7 proprietary

G.703, 75 ohm Interface at the main unit (G703-75-4CH module)

Bit rate	2048 kbit/s +/- 50 ppm
Code	HDB3 (*G.703* Annex A)
Nominal impedance	75 ohm unbalanced
Pulse shape	*G703* Figure 15
Nominal peak voltage	2.37 V (75 ohm)
Nominal pulse width	244 +/- 25 ns
Attenuation margin	6 dB at 1024 kHz
Input return loss	*G.703* § 6.3.3
Output return loss	*ETS 300 166* § 5.3
Jitter tolerance	*G.823* § 3.1.1
Output jitter when transmit signal timing is supplied by the unit operating in the internal mode	< 0.05 UI (20 Hz…100 kHz)
Output jitter when the node is synchronized from an G703-75-4CH interface or the external clock input interface	*TBR 12* § 5.2.1.4 *TBR 13* § 5.2.1.4
Output short circuit current	< 50mA RMS
Connector type	SMB (unbalanced 75 ohm)
Overvoltage Protection	*G.703* Annex B

G.703 120 ohm Interface at the main unit (G703-120-4CH module)

Bit rate	2048 kbit/s +/- 50 ppm
Code	HDB3 (*G.703* Annex A)
Nominal impedance	120 ohm balanced
Pulse shape	*G703* figure 15
Nominal peak voltage	3.0 V (120 ohm)
Nominal pulse width	244 +/- 25 ns
Attenuation margin	6 dB at 1024 kHz
Input return loss	*G.703* § 6.3.3
Output return loss	*ETS 300 166* § 5.3
Jitter tolerance	*G.823* § 3.1.1
Output jitter when transmit signal timing is supplied by the unit operating in the internal mode	< 0.05 UI (20 Hz…100 kHz)
Output jitter when node is synchronized from an G703-120-4CH interface or external clock input interface	*TBR 12* § 5.2.1.4 *TBR 13* § 5.2.1.4
Connector type	D-type 9-pin female connector
Overvoltage Protection	*G.703* Annex B

G.703 75 ohm Interface at the optional interface card (G703-75 module)

Bit rate	2048 kbit/s +/- 50 ppm
Code	HDB3 (*G.703* Annex A)
Nominal impedance	75 ohm unbalanced
Pulse shape	*G.703* figure 15
Nominal peak voltage	2.37 V (75 ohm)
Nominal pulse width	244 +/- 25 ns
Attenuation margin	6 dB at 1024 kHz
Input return loss	*G.703* § 6.3.3
Output return loss	*ETS 300 166* § 5.3
Jitter tolerance	*G.823* § 3.1.1
Output jitter when transmit signal timing is supplied by the SXU operating in the internal mode	< 0.05 UI (20 Hz…100 kHz)
Output jitter when the node is synchronized from an G703-75 interface or SXU external clock input interface	*TBR 12* § 5.2.1.4
Output short circuit current	< 50mA RMS
Connector type	SMB (unbalanced 75 ohm)

G.703 75 ohm Interface at the optional interface card (G703-120 module)

Bit rate	2048 kbit/s +/- 50 ppm
Code	HDB3 (*G.703* Annex A)
Nominal impedance	120 ohm balanced
Pulse shape	*G.703* figure 15
Nominal peak voltage	3.0 V (120 ohm)
Nominal pulse width	244 +/- 25 ns
Attenuation margin	6 dB at 1024 kHz
Input return loss	*G.703* § 6.3.3
Output return loss	*ETS 300 166* § 5.3
Jitter tolerance	*G.823* § 3.1.1
Output jitter when transmit signal timing is supplied by the SXU operating in the internal mode	< 0.05 UI (20 Hz…100 kHz)
Output jitter when the node is synchronized from an G703-120 interface or SXU external clock input interface	*TBR 12* § 5.2.1.4
Connector type	D-type 9-pin female connector

G.703 8Mbit/s Interface (G703-8M Module)

Bit rate	8448 kbit/s ± 30 ppm
Code	HDB3 (*G.703* Annex A)
Nominal impedance	75 ohm unbalanced
Pulse shape	*G.703* figure 16
Nominal peak voltage	2.37 V (75 ohm)
Nominal pulse width	59 ± 10 ns
Attenuation margin	6 dB at 4224 kHz
Input return loss	*G.703* § 7.3.3
Jitter tolerance	*G.823* § 3.1.1
Output jitter when transmit signal timing is supplied by the SXU operating in the internal mode	< 0.05 UI (20 Hz…400 kHz)
Connector type	SMB (unbalanced 75 ohm)

2048 kbit/s Long-haul Interface (LTE Module)

Bit rate	2048 kbit/s +/- 50 ppm
Code	HDB3 (*G.703 Annex A*)
Nominal impedance	120 ohm balanced
Pulse shape	*G.703 Figure 15*
Nominal peak voltage	3.0 V (120 ohm)
Nominal pulse width	244 +/- 25 ns
Attenuation margin	36 dB at 1024 kHz
Return loss	*G.703 § 6.3.3*
Jitter tolerance	*G.823 § 3.1.1*
Output jitter when transmit signal timing is derived from the SXU operating in the internal mode	< 0.05 UI (20 Hz ...100 kHz)
Connector type	D-9 (balanced 120 Ohm)
Overvoltage protection	Gas discharge tubes, diodes

1088 kbit/s Long-haul Interface (LTE Module)

Bit rate	1088 kbit/s +/- 50 ppm
Code	HDB3 (*G.703 Annex A*)
Nominal impedance	120 ohm balanced
Pulse shape	Rectangular
Nominal peak voltage	3.0 V (120 ohm)
Nominal pulse width	460 +/- 40 ns
Attenuation margin	36 dB at 544 kHz
Return loss	*G.703 § 7.3.3*

Jitter tolerance	*G.823 § 3.1.1* with following exceptions:	
	A0	19.6 (18 µs)
	A1	0.75
	A2	0.10
	F4	50 kHz

Output jitter when transmit signal timing is derived from the SXU operating in the internal mode

	< 0.05 UI (20 Hz…50 kHz)
Connector type	D-9 (balanced 120 ohm)
Overvoltage protection	Gas discharge tubes, diodes

592 to 2320 kbit/s HDSL Line Interface (HCE Modules)

Module type	HCE-2M-2P	HCE-2M-1P
Line rate kbit/s	592	592
	1168	1168
		2320

Connection	1 or 2 pairs full duplex with echo cancellation
Impedance	135 ohms
Send level range	13.5 dBm @ 135 ohms
Return loss	>16 dB from 40 kHz to 292 kHz for HCE-2M-2P >16 dB from 40 kHz to 485 kHz for HCE-2M-1P
Common mode rejection	>50 dB from 5 kHz to 292 kHz for HCE-2M-2P >50 dB from 5 kHz to 485 kHz for HCE-2M-1P
Signal encoding	2B1Q
Overvoltage protection	PTCs, gas discharge tubes, diodes
Signal monitoring	1. carrier detection
	2. received signal noise margin
	3. received signal level monitoring
Connector type	D-9 (balanced 120 ohm)
Overvoltage protection	Gas discharge tubes, diodes

2048 kbit/s Fibre Optical Interface (OTE-LED and OTE LP Modules)

Bit rate	2048 kbit/s +/- 50 ppm
Code	CMI
Symbol rate	4096 kbaud
Pulse shape	Rectangular
Transmission path	Standard single-mode fiber (*ITU-T G.652*) Standard multimode fiber (*ITU-T G.651*)
Optical transmitter	Semiconductor LED or LASER diode
Optical receiver	PIN-diode
Nominal wave length	1300 nm
Minimum output power to multimode fiber	
	OTE-LED: -20 dBm
	OTE-LP: -2 dBm
Minimum output power to single mode fiber	
	OTE-LED: -30 dBm
	OTE-LP: -4 dBm
Receiver sensitivity (BER 10^{-9})	-50 dBm
Connector type	FC-type with receptacle

8448 kbit/s Fibre Optical Interface (OTE-LED and OTE LP Modules)

Bit rate	8448 kbit/s +/- 30 ppm
Code	CMI
Symbol rate	16896 kbaud
Pulse shape	Rectangular
Transmission path	Standard single-mode fiber (*ITU-T G.652*) Standard multimode fiber (*ITU-T G.651*)
Optical transmitter	Semiconductor LED or LASER diode
Optical receiver	PIN-diode
Nominal wavelength	1300 nm
Minimum output power to multimode fiber	
	OTE-LED: -20 dBm
	OTE-LP: -2 dBm
Minimum output power to single mode fiber	
	OTE-LED: -30 dBm
	OTE-LP: -4 dBm
Receiver sensitivity (BER 10^{-9})	-42 dBm
Connector type	FC-type with receptacle

Note: In case of an optical laser transmitter, the maximum input power allowed to the receiver is -15 dBm. In case of trouble the advise is to measure the power using a commercial optical power meter. However, if this meter is not available and the only fact to base the decision on is the transmission distance, the following rule of thumb applies:

If the fiber is multimode fiber (G.952) or standard single mode fiber, the minimum distance should be 15 km if OTE-LP is intended to be used. This depends strongly on the attenuation of the fiber and used splicing and cabling techniques and should always checked with the customer.

Transport Module (TM) Clock Jitter and Wander

Output jitter, measured within the frequency range 20 Hz to 100 kHz	
2 Mbit/s and clock port output, internal timing	0.05 UIp-p max.
2 Mbit/s port output, Transport Module (node) synchronised from an external clock at 2048 kHz containing no jitter	0.05 UIp-p max.
2 Mbit/s port output, Transport Module (node) synchronised from an interface at 2 Mbit/s containing no jitter	0.10 UIp-p max.

Input jitter tolerance at the external clock interface at 2048 kHz
See 7.1 (G.823 fig. 3)

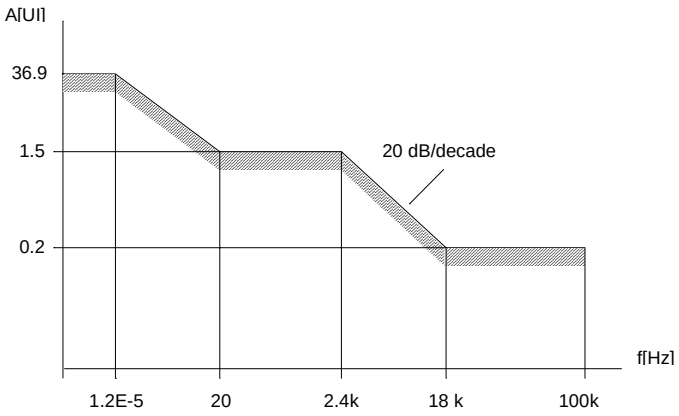


Fig. 7.1: Input Jitter Tolerance for the External Clock

Jitter transfer function from 2 Mbit/s port A to 2 Mbit/s port B or
from an external clock at 2048 kHz to a 2 Mbit/s port

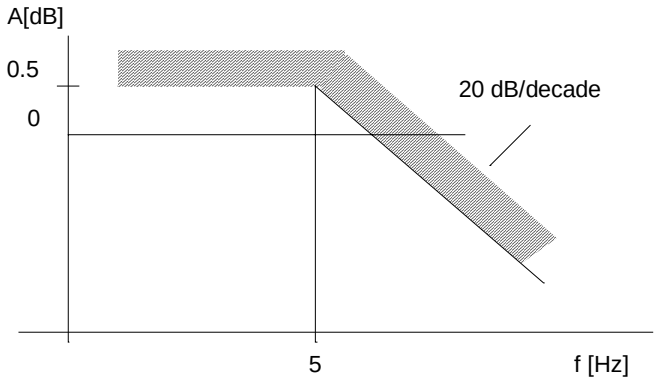


Fig. 7.2: Jitter Transfer Function

Frame and Multiframe Operation

Filtering of FEA and MFrFEA bit:
The state of the alarm bit will switch if the opposite state is received three times consecutively.

AIS in frame 2048 kbit/s and n x 64 kbit/s:
Signal containing two or less zeros in a 2-frame period is recognised as an AIS signal.
After AIS is detected, a signal containing three or more zeros in a 2-frame period is recognised not to be an AIS signal.

AIS in frame 8448 kbit/s:
A signal containing less than eight zeros in a 2-frame period is recognised as an AIS signal. After AIS is detected a signal containing 12 or more zeros in a 2-frame period is recognised not to be an AIS signal.

AIS in multiframe:
A signal in the signalling time slots containing one or no zeros in a multiframe period is recognised as an AIS signal.

Error rate 10E-3 limits from frame alignment word:

2048 kbit/s and n x 64 kbit/s count time is four seconds	
Count to activate alarm:	94
Count to inactivate alarm:	17
8448 kbit/s count time is 2 seconds	
Count to activate alarm:	199
Count to inactivate alarm:	48

Error rate 10E-3 limits from code errors:

Count time is one second

Speed kbit/s	Activate	Inactivate
8448	8296	893
2048	1973	229
1088	1033	126

CRC spurious frame alignment limits:

speed kbit/s	values from 1000 counted to start a new frame search
256	613
320	637
384	660
448	681
512	700
576	719
640	736
704	753
768	768
1088	832
2048	915
8448	826

Power Supply

The power requirements depend on type of interface at the optional interface card the line speed, and the actual alarm status. The power consumption is approximately as shown in the table below.

Plug-in unit- without optional interface card:	< 8.4 W
Plugin-unit with optional card and two interfaces:	
G703 at 2 Mbit/s	< 14.2 W
G703 at 8 Mbit/s	< 15.6 W
LTE at 2 Mbit/s	< 14.2 W
HCE 2 pair x1 Mbit/s	< 16.4 W
OTE-LED at 8 Mbit/s	< 19.4 W
OTE-LP at 8 Mbit/s	< 22.4 W

Mechanics

Weight:	
Plug-in unit without optional interface card	2.3 kg
Plug-in unit with optional interface card	3.0 kg
Size:	
Sub-rack dimensions (HxWxD):	245x70x228 mm
Unit dimensions:	25 x 160 x 233 mm
Environmental conditions:	
Temperature.	+5 .. +45 C
Humidity	< 85%, RH

Appendix

Frame structures and buffers

2048 kbit/s Frame Structure

The DXX system utilises a frame structure for 2048 kbit/s according to *G.704*. The first time slot of a frame, **ts0**, contains the **Frame Synchronization Word (FSW)**. The bits of this frame synchronization word have a different meaning in odd and even frames. Even frames contain the frame alignment signal and odd frames specify one bit of this word as a frame alignment signal, one bit as the far-end alarm bit and five special bits. Four of these five special bits are recommended to be used by the internal HDLC channel of the DXX system. The function of these bits is defined in the user interface through the **GMH Parametrization** window. However, if CRC check is used, then the first bit in time slot ts0 of every frame is used by the CRC check and cannot be defined for other purposes in the user interface.

The first bit of 16 consecutive time slots ts0 form a CRC multiframe consisting of 16 frames. This multiframe has six frame synchronization bits, eight bits for the CRC check sum, and two bits used to transmit far-end block error information. The period of 16 frames is divided into two subgroups, each consisting of eight frames. A check sum is separately calculated for both subgroups and sent during the next subgroup. The receiving end performs the CRC check, and if a faulty block is detected, then information about this is sent to the far-end by setting the corresponding block error bit to state **0** during one multiframe.

Time slots ts1…ts15 and ts17…ts31 are reserved for payload data transmission. Each data time slot has a corresponding 4-bit signalling word, which is transmitted in time slot ts16 of a multiframe. The bits in time slot ts16 can be utilised by other functions if no signalling capacity is required by a data time slot.

The length of a multiframe is 16 frames. Within the multiframe the first ts16 time slot (in the first frame) is used to transmit the multiframe synchronization word (four bits in the **0** state), the multiframe far-end alarm and three special bits. The function of the special bits can be defined through the user interface. It is recommended to set these bits in state **1** when they are not used. The ts16 time slots of the other frames carry signalling data for two time slots each, four bits for each data time slot. For example, ts16/Fr1 carries signalling data for the time slots ts1 and ts17.

An HDLC channel can be placed in any free time slot where it can occupy a required number of bits. A time slot bit can carry 8 kbit/s of data, and thus the total capacity of the 8 bits in a time slot is 8 x 8 = 64 kbit/s. It is, however, recommended to locate the HDLC channel in the bits B5, B6, B7 and B8 of the time slot ts0. Due to the frame alternation the time slot TS0 capacity is only 4 kbit/s per bit, and these four bits together provide a 16 kbit/s transmission channel. If the HDLC channel is located in bit B1 of time slot ts0, replacing the CRC check, then no other bits can be used to form the HDLC channel.

N x 64 kbit/s Frame Structure

The n x 64 kbit/s frame structure is a modified 2048 kbit/s frame structure. A frame is again repeated with the frequency 8 kbit/s, as with other transmission speeds, but because the transmission speed is now lower, the frame must be shorter. The modified frame consists of n time slots to be transmitted. The time slot ts0 has the same structure as for 2048 kbit/s, and the frame special bits and CRC check have the same function as for 2048 kbit/s. The signalling multiframe is constructed in the same way as for 2048 kbit/s, but now the last time slot in a frame is used for signalling purposes.

Frame Multiplexing and Demultiplexing at 2048 kbit/s
A frame to be transmitted is multiplexed in the Frame Mux and clocked by the Tx clock. The data to be transmitted is received through the X-bus into a transmit buffer, from which the Frame Mux fetches data, one time slot at a time, controlled by the bus frame clock. The time slot ts0 can also be received via the transmit buffer from the bus, but usually the frame alignment signal is generated in the Mux. The other bits for the ts0 are read into the transmitted frame from positions defined through the user interface. E.g. the HDLC channel data is received from the HDLC controller in serial form and clocked by the Tx clock. The data for the first frame in the signalling multiframe is generated in the Mux and the time slot signalling data is received via the transmit buffer from the X-bus. Before the frame is transmitted, a CRC check sum is calculated and the CRC multiframe structure is placed into the first bit of time slot ts0.

The receiver will search for the frame alignment signal in the received decoded signal. When the alignment is found at the correct position in consecutive frames, the receiver is synchronized and the frame demultiplexed. The frame alignment search is performed in accordance with a state diagram which should ensure that the receiver will be correctly synchronized even on noisy connections.

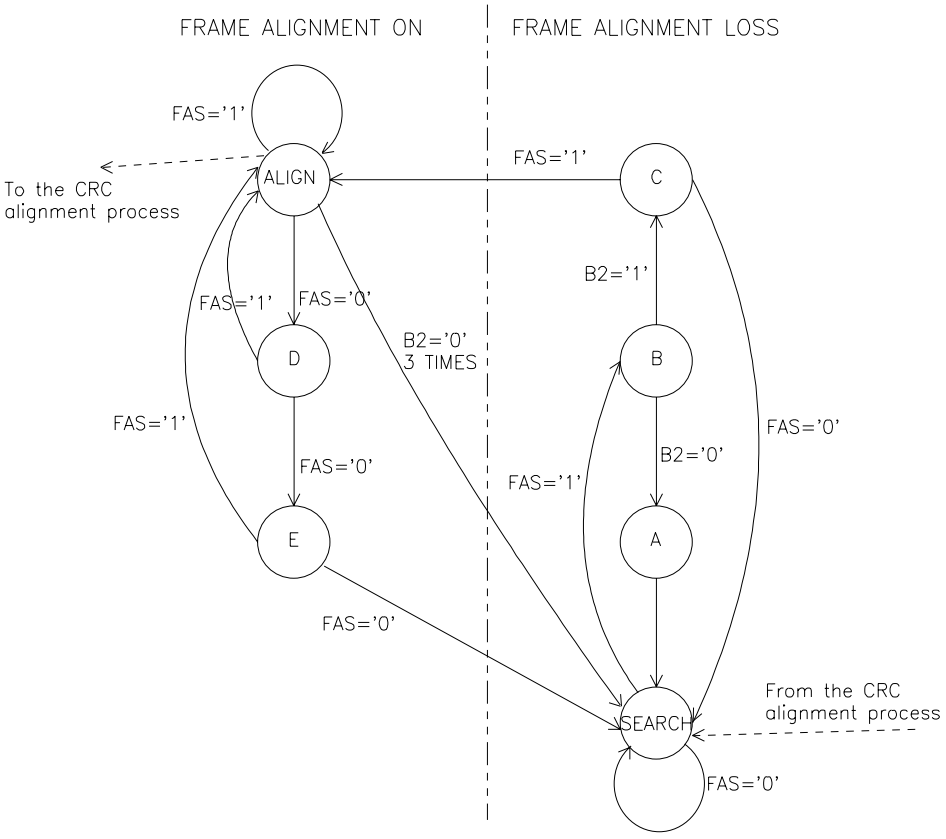


Fig. 0-2: Frame Alignment State Diagram at 2048 kbit/s

The right-hand side of figure 4.1-8 shows the states in the search mode: the frame alignment alarm is activated and the data to the X-bus is set to AIS. On the left-hand side the receiver is synchronized to a received frame and the alarm is inactive. In the search mode the correct frame synchronization word must be found, thereafter the time slot ts0 in the next frame must have the bit B2 in state **1**, then the frame synchronization word again has to be in the correct position in the next frame, and only then the frame is synchronized. If any of these conditions is not fulfilled, the search is repeated from the beginning. When the frame is synchronized, the frame alarm is inactivated and at the same time the AIS is removed from the data supplied to the X-bus.

When the frame alignment is found, the receiver monitors the received frame synchronization words. The frame alignment is considered lost if a corrupted frame synchronization word is received in three consecutive frames. In this case the frame synchronization alarm is activated and a new frame alignment search is started. The receiver monitors also the state of bit B2 in time slot ts0 of odd frames. The frame alignment is considered lost if the bit B2 is **0** in three consecutive frames

The number of faulty frame synchronization words is also counted in the receiver in order to calculate the error rate of the connection. Normally, the error rate limit is set to 10E-3. If the error rate exceeds this value, the reception is inhibited and the receiver sets AIS as data to the X-bus and activates the error rate alarm. The error rate is not calculated when the frame alignment is lost.

The state of the received data bits is monitored in order to detect an AIS. The received data is considered to be AIS if there are less than three bits in state **0** during two frames and a corresponding alarm is activated. The far-end alarm bit is extracted from time slot ts0 in a received frame. The alarm bit is filtered so that three identical states in consecutive frames are required to change the filtered value. A filtered value **1** activates the functions defined in the alarm table.

In receiver fault situations - if the error rate is too high or if the frame alignment is lost, for instance - the receiver transfers corresponding information to the transmitter which then activates the far-end alarm bit in the transmitted time slot ts0.

The CRC check is used to increase the reliability of frame alignment and to prevent alignment on words only simulating the frame synchronization word. The receiver is synchronized to the first word found to be identical with the frame synchronization word. If this detected word is sent by some data equipment in a data slot and if this word remains the same for a longer period, the receiver can falsely synchronize to this simulating synchronization word. This situation is detected with the CRC check.

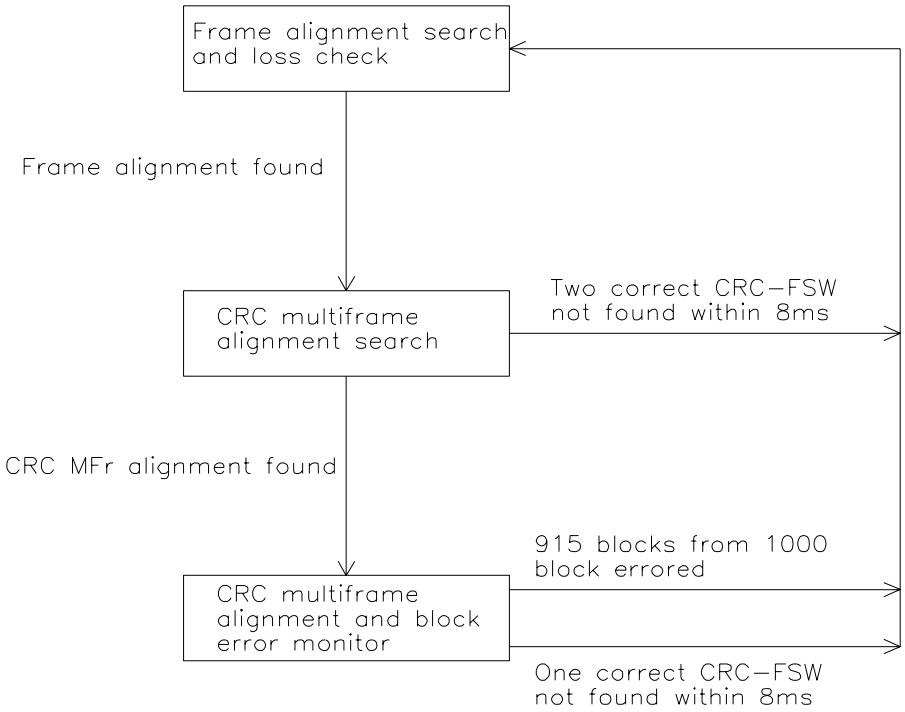


Fig. 0-3: CRC Multiframe Alignment State Diagram at 2048 kbit/s

The CRC multiframe alignment state diagram is shown in Fig. 0-3. The state at the top contains the 2048 kbit/s frame alignment state diagram. When frame alignment is found, the receiver starts the search for the CRC multiframe alignment signal. The CRC multiframe alignment is found when the receiver finds two correct CRC multiframe alignment signals in the correct position within a period of 8 ms. Then the CRC error count is started. If two CRC multiframe alignment signals are not found within the period of 8 ms, then also a new frame alignment search is started and a frame synchronization alarm is activated.

The receiver starts to count CRC block errors when the CRC multiframe alignment is found. The frame alignment search is started and an alarm is activated if there are more than 914 faulty blocks out of 1000 blocks. The CRC multiframe synchronization words are also monitored: if no correct CRC multiframe synchronization word is found within 8 ms, then a new frame alignment search is started.

The signalling multiframe consists of the time slots ts16 of 16 consecutive frames. The first four bits of time slot ts16 in the first frame form the multiframe synchronisation word. These bits are all zeroes (**0**). The other time slots ts16 contain signalling information for the data time slots.

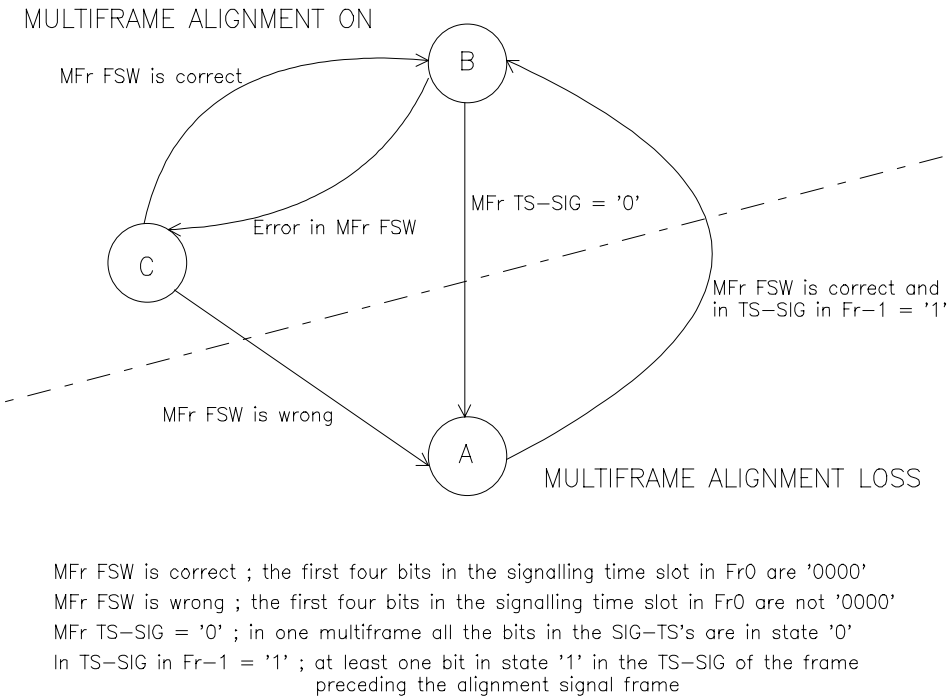


Fig. 0-4: Signalling Multiframe Alignment State Diagram

The signalling multiframe alignment signal search begins when the frame alignment is found. When the first four bits of time slot ts16 are found to be zeroes (**0**), this is considered to be the multiframe synchronisation word. However, in order to avoid a false alignment it is required that the prior time slot ts16 had at least one bit in state **1**. The AIS is removed from the signalling information to the X-bus and the multiframe alarm sent to the far-end is inactivated when the alignment is found.

The multiframe synchronization word monitoring function is started when the multiframe is synchronized. If errors are found in two consecutive synchronization words, the multiframe alignment is considered to be lost. In the synchronized state the contents of all time slots ts16 are monitored, and if all time slots ts16 in one multiframe contain only zeroes (**0**) the multiframe alignment is considered to be lost. A corresponding alarm is activated if the alignment is lost, the signalling data to the X-bus is set to AIS and the transmitted far-end alarm is activated (ts16/B6).

The far-end alarm is extracted from the received signalling multiframe synchronization time slot. The alarm state is filtered so that three identical states in consecutive frames are required to change the filtered value. A filtered value **1** activates an alarm. Through the user interface it is possible to define that the alarm state also puts the signalling data to the X-bus to AIS. In such case the frame far-end alarm bit will also put the signalling data directed to the X-bus to AIS.

If the signalling multiframe synchronization is lost, the received signalling time slot data is monitored in order to detect an AIS. A signal is considered to be AIS if the signalling time slot during one multiframe contains only one bit or no bits in state **0**.

Frame Assembling and Disassembling at n x 64 kbit/s
A frame is assembled and disassembled at n x 64 kbit/s in a similar way to that of 2048 kbit/s. The minor differences are due to the smaller number of bits in the frame.

A different number of faulty frame synchronization words is required in the error rate count to trigger an alarm and to inactivate it.

The number of CRC block errors required to start a new search for the frame alignment depends on the transmission speed. The number decreases when the transmission speed is lowered.

The signalling frame time slot is the last time slot in a frame. Multiframe alignment is achieved in the same way as at 2048 kbit/s.

8448 kbit/s Frame Structure

The DXX system uses a frame structure in accordance with *G.704* at 8448 kbit/s. The frame contains 132 time slots of eight bits each, and thus the frame length is 1056 bits. The frame is repeated at a frequency of 8 kHz. The frame synchronization word (FSW) consists of 14 bits and it is divided into two time slots: eight bits in time slot ts0 and six bits in time slot ts66. The time slot ts66 also contains a frame level far-end alarm bit and one special bit (ts66/B8). The use of this special bit can be defined via the user interface.

CRC6 checkbits are located in time slot ts99. The first six bits are reserved for the transmission of the calculation results, the bit B7 is the far-end block error bit and the use of the bit B8 can be defined through the user interface. The CRC check uses no multiframe, but the check sum is always calculated for each frame and sent in the next frame. If an error is detected in the received block, corresponding information is sent to the far-end by setting the transmitted bit B7 to **1** during one frame.

Time slots ts5…ts32, ts34…ts65, ts71…ts98 and ts100…ts131 of a frame are reserved for data transmission. Signalling capacity is reserved for each data time slot in the signalling multiframes defined by time slots ts67…ts70. The data time slots are divided into four groups, Gr1…Gr4. Each signalling group contains 30 time slots and has an individual signalling time slot, which is independently processed. The multiframe structure and the synchronization time slot are similar to those used at 2048 kbit/s.

It is possible to use the time slots ts1…ts4 and TS33 for data transmission, but there is no defined signalling capacity for these time slots.

It is recommended that the HDLC channel is located in time slot TS33 or in TS1, which gives this channel a capacity of 64 kbit/s. For special purposes the HDLC channel position can be put in any time slot through the user interface, through which it is also possible to select any of the time slot bits 1…8 to be used by the HDLC channel.

Frame Multiplexing and Demultiplexing at 8448 kbit/s

A frame for 8448 kbit/s is assembled in the same way as for 2048 kbit/s. The data is received via the X-bus and inserted, clocked with the Tx clock, into the time slots of the frame to be transmitted. Frame synchronization words are generated or extracted from the transmit buffer, special bits are set at their positions, and, eventually, the CRC check sum for the whole frame is calculated and inserted into the transmitted frame in an individual time slot.

A frame alignment signal search is performed on the received decoded line signal. When the alignment is found, the receiver is synchronized to the received frame clock in a defined sequence.

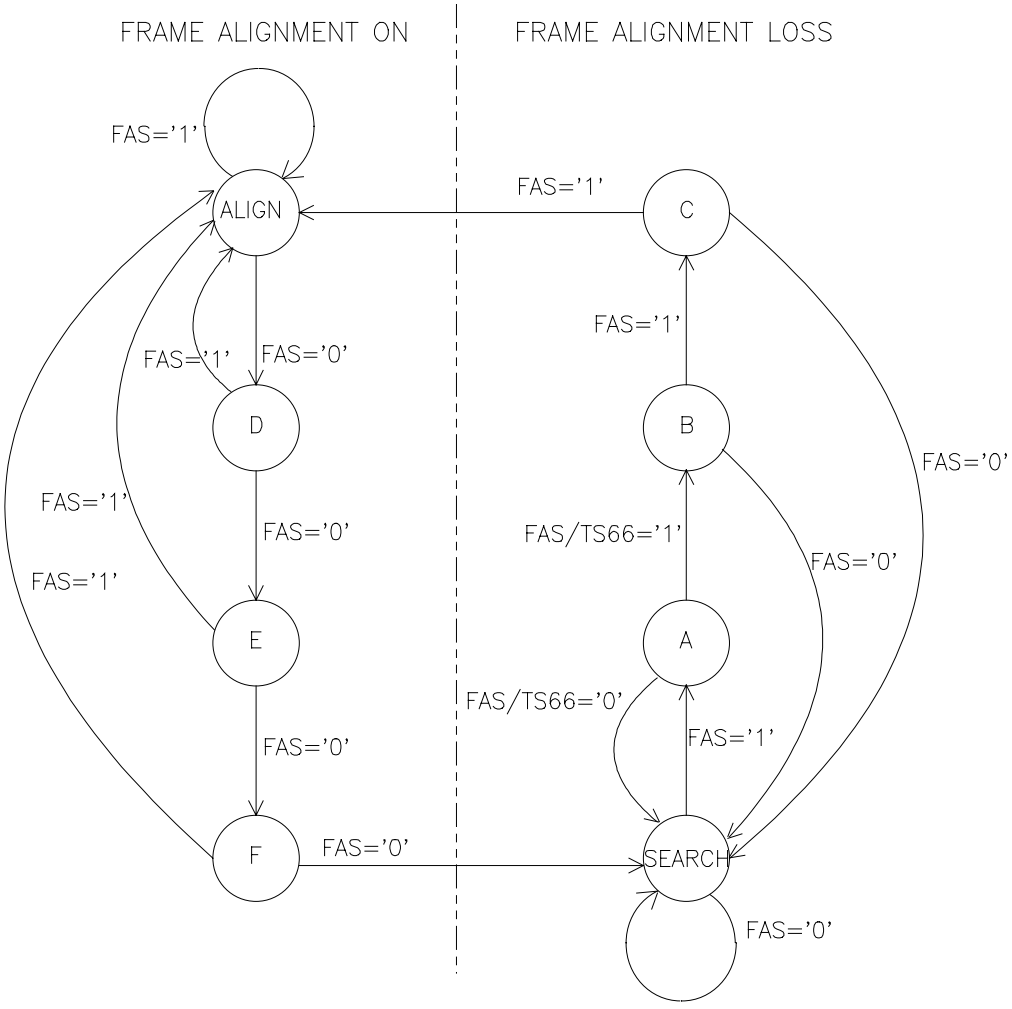


Fig. 0-5: Frame Alignment State Diagram at 8448 kbit/s

A frame alignment sequence is shown in Fig. 0-5, on the left side, where the receiver is synchronized to the received signal. The right-hand side of the figure shows the alignment loss sequence.

The frame alignment is found when the whole frame synchronization word in three consecutive frames is received without errors at the correct position. The frame alignment is considered lost if a corrupted frame synchronization word is received in four consecutive frames. In this case the frame synchronization alarm is activated and AIS is set as data to the X-bus.

The receiver counts the number of faulty frame synchronization words when synchronization is achieved. Frame synchronization word bits in time slot ts0 and time slot ts66 are counted. The number of faulty frame synchronization words is used to calculate the error rate of the connection. If the error rate exceeds 10E-3, the receiver sets AIS as data to the X-bus and activates the error rate alarm.

The state of the received data bits is monitored in order to detect an AIS. The received data is considered to be AIS if there are seven or fewer bits in state **0** during two frames and a corresponding alarm is activated. If the alarm is activated, at least 12 bits have to be activated in state **0** during two frames before the alarm is inactivated.

The far-end alarm bit is located in bit B7 of time slot ts66. The alarm bit is filtered so that three identical states in consecutive frames are required to change the filtered value. In the transmitter end the far-end alarm bit is activated in accordance with the situations defined in the alarm table, i.e. when there is a serious frame level fault in the Rx direction.

The CRC6 check is used to increase the reliability of frame alignment and to monitor the error rate of the data transmission. The number of blocks with errors is counted when the synchronization is achieved. If there are more than 825 faulty blocks out of 1000 blocks, the frame is not correctly synchronized and a new search is started. The CRC6 check is well suited to monitor low error rates.

Each signalling multiframe of the time slots ts67, ts68, ts69 and ts70 is independent. The alignment sequences and the multiframe construction are the same as for a 2048 kbit/s frame.

Buffers and Buffer Handling

In the transmitting direction the buffer supplies time slot data from the X-bus to the frame to be transmitted. When the cross-connect unit supplies data to the X-bus, it also adds information about the location in the transmitted frame where the data is to be placed. The unit stores the data in its transmit buffer in a position corresponding to the time slot's position in the frame. The frame multiplexing circuits will fetch the data when they are transmitting the corresponding time slot. As it is possible to write the data from the bus to any time slot position in the buffer, the buffer must control that write and read operations do not simultaneously address the same time slot. In the GMH unit there are two ways to avoid such conflict situations:

1. The transmit buffer length is set to two frames. Then the frame multiplexing block reads the first frame area and the bus writes into the second frame area. This transmit buffer arrangement causes a delay of one frame or 125 μs.

2. The read and write operations are performed on the same frame area, but the transmitted frame is synchronized to the bus frame clock and data is written to the buffer in a defined sequence and at a regular speed so that a read/write conflict is effectively prevented. In this case there is only a small frame delay, but the data must be evenly distributed in time slots on the X-bus. The bus has a limited capacity for even distribution: it is reserved for 2048 kbit/s and 8448 kbit/s connections, and it is recommended to use this capacity for trunk lines.

Through the user interface the **Rx Buffer** can be set to the **2 Fr** alternative. In this case the transmit buffer is set to the short form which provides a short delay. The other alternatives create a two-frame buffer.

In the receiving direction the buffer supplies received time slot data from the demultiplexed frame to the X-bus. When the cross-connect unit requests data from the interface units through the X-bus, it also specifies the time slot concerned. Usually, the phase of the received frame does not coincide with the frame phase of the X-bus; on the other hand, the receiver writes time slot data into the Rx buffer clocked by the received frame. Therefore the Rx buffer has to control that the read and write operations do not collide, in spite of speed fluctuations and jitter. If the read and write addresses come too close, one of them has to be moved, i.e. centred. The allowed minimum distance between the read and write addresses depends on the system requirements. In the GMH unit the centring is made by changing the read address, the change being always one frame or a multiple of a frame. The centring causes a certain number of frames to be lost or re-transmitted; the number is proportional to the distance which the read address is moved. Through the user interface it is possible to select four different lengths for the receiving buffer, in order to meet different requirements, such as a minimum delay or the ability to tolerate large speed fluctuations.

Centring is required when the equipment is powered up, when a received signal contains disturbances, or when the transmission is plesiochronous. If a plesiochronous system constantly exhibits a frequency difference in the same direction, the buffer has to be centred at regular intervals. The length of the interval depends on the frequency difference and on the distance from the centred read address position to the position where a new centring occurs.

Operating Modes of Buffers			
Rx Buffer	Rx delay	Tx length	Tx delay
2 Fr	0…2 Fr	1 Fr	approx. 0 Fr
4 Fr	1…3 Fr	2 Fr	1 Fr
8 Fr	1…7 Fr	2 Fr	1 Fr
8 Fr Split trunk	2…6 Fr	2 Fr	1 Fr
64 Fr	1…63 Fr	2 Fr	1 Fr

2 Fr Rx Buffer
The length of the receiving buffer is two frames, which provides a minimum connection delay.

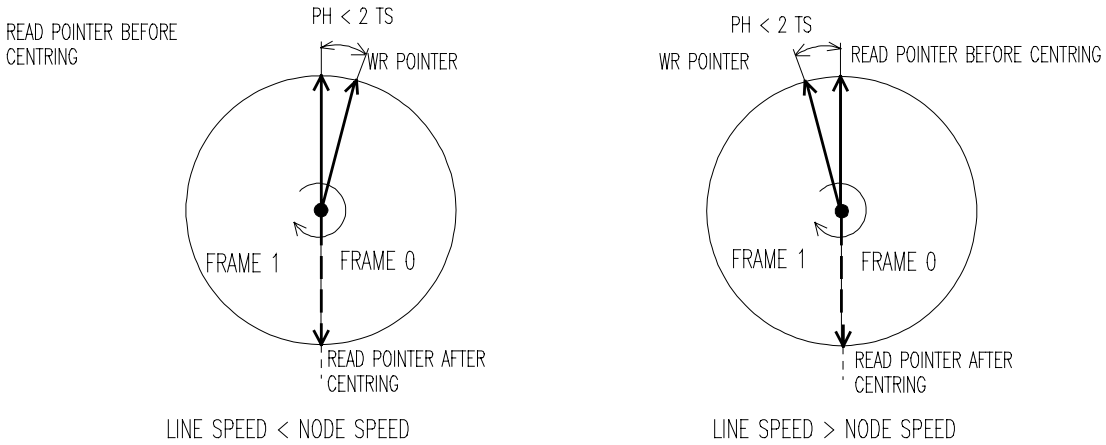


Fig. 0-6: Centring in an Rx Buffer of Two Frames

In a short buffer the minimum allowed distance between the read and write addresses is one time slot. The distance is checked at intervals of two frames when the read address moves to a new frame. If the addresses are too close at the checking time, a centring is performed by moving the read address one frame further. This means that one frame is either lost or repeated once. In a plesiochronous system the distance from the centred position to the position where a new centring occurs is one frame as in Fig. 0-6, and the interval between the centring situations is:
at 2048 kbit/s 240/df
at 8448 kbit/s 1024/df

where **df** is the frequency difference between the signal received from the line and the receiving frequency generated by the X-bus clock frequency.

The short buffer can be used for 2048 kbit/s and 8448 kbit/s connections, and then an even distribution is used on the X-bus. This is recommended for trunk lines in order to keep the transmission delays as short as possible.

4 Fr Rx Buffer

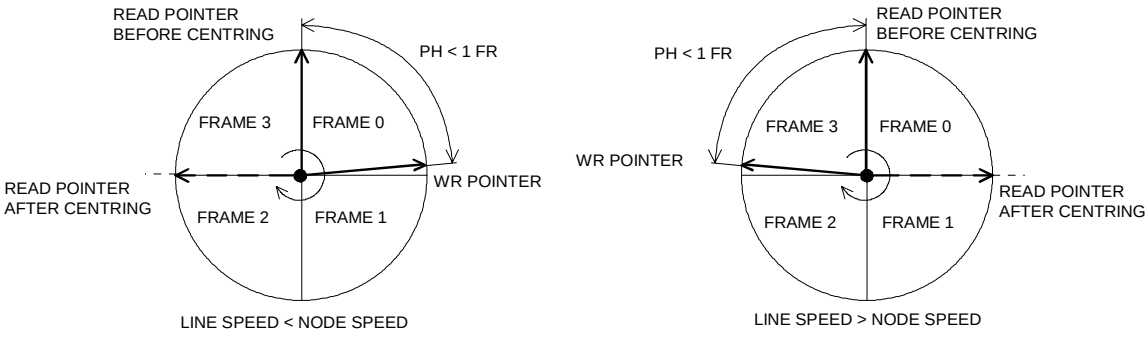


Fig. 0-7: Centring in an Rx Buffer of Four Frames

The minimum allowed distance between the read and write addresses is one frame. The distance is checked at intervals of four frames when the read address moves to frame Fr0 (from the frame Fr3). If the addresses are too close at the checking time, a centring is performed by moving the read address one frame further. The address jump direction depends on the direction from which the write address was closing in on the read address. Centring means here that one frame is either lost or repeated once. In a plesiochronous system with a four-frame Rx buffer the interval between centring situations is:
at n x 64 kbit/s n x 8/df
at 2048 kbit/s 256/df
at 8448 kbit/s 1056/df

It is recommended that the **4 Fr** buffer is used for framed user interfaces and for n x 64 kbit/s trunk lines.

8 Fr Rx Buffer

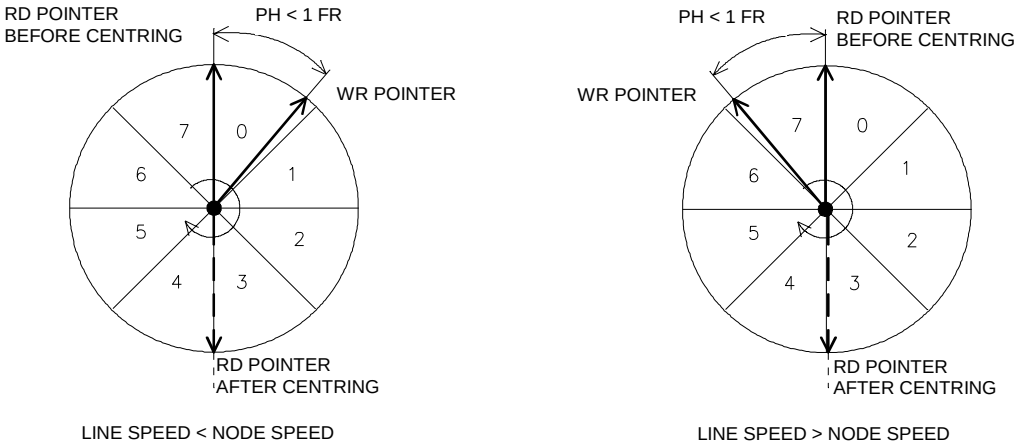


Fig. 0-8: Centring in an Rx Buffer of Eight Frames

The allowed distance between read and write addresses in an Rx buffer of eight frames is one frame. If a shorter distance is detected by the check, then the read address is moved to a new position four frames farther away. In this case centring means that four frames are either lost or repeated once. The eight frames buffer retains the frame alternation also after the cross-connect, when a 2048 kbit/s framing structure or a n x 64 kbit/s framing structure is used.

The **8 Fr** buffer is the only possibility for **Split Trunks**. The centring for **Split Trunks** is defined so that the minimum allowed distance between the read and write addresses is two frames. In other respects the centring is equal to the 8-frame buffer's basic mode.

In a plesiochronous system the interval between centring situations is:

at n x 64 kbit/s	4 x n x 8/df
at n x 64 kbit/s **Split Trunk**	2 n x 8/df
at 2048 kbit/s **Split Trunk**	512/df
at 2048 kbit/s	1024/df
at 8448 kbit/s	4224/df

A buffer with a length of eight frames is used for **Split Trunk** operation. It may also be used for other applications, in particular if unusually large fluctuations have to be handled correctly or if the frame alternation has to be intact also after the centring.

64 Fr Rx Buffer

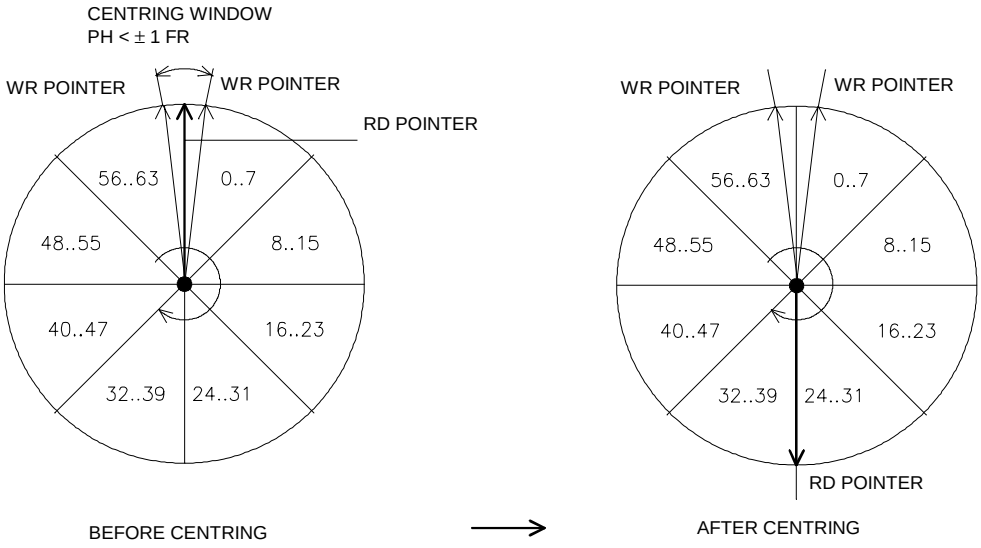


Fig. 0-9: Centring in an Rx Buffer of 64 Frames

In an Rx buffer of 64 frames a new centring is triggered if the distance between the read and write addresses is less than one frame. Centring means now that 32 frames are either lost or repeated once. The long buffer leads to a delay of up to 63 frames and thus this buffer mode is recommended for special purposes only. The slip distance is very large in a plesiochronous system and the buffer is well suited for large frequency fluctuations. This buffer mode can be used at 2048 kbit/s and n x 64 kbit/s.
In a plesiochronous system the interval between centring situations is:

at n x 64 kbit/s 32 x n x 8/df

at 2048 kbit/s 8192/df

Multiframe Buffers
In the transmitting direction the signalling data is directed through the same buffer as the time slot data. The signalling multiframe of the frame to be transmitted is synchronized to the multiframe clock of the X-bus. The cross-connect unit supplies frame signalling data together with other time slot data of the frame. The GMH unit generates a synchronization time slot in the first frame of the signalling multiframe. Thus the signalling data and time slot data have equal delays in the transmitting direction.

In the receiving direction the phase of the received signal multiframe usually differs from the phase of the X-bus multiframe. Thus the received signalling data has to be buffered until the cross-connect unit performs the cross-connect function for the concerned data. There are two alternatives for the multiframe buffer length: two and four multiframes. The multiframe buffer length depends on the selected length of the frame buffer.

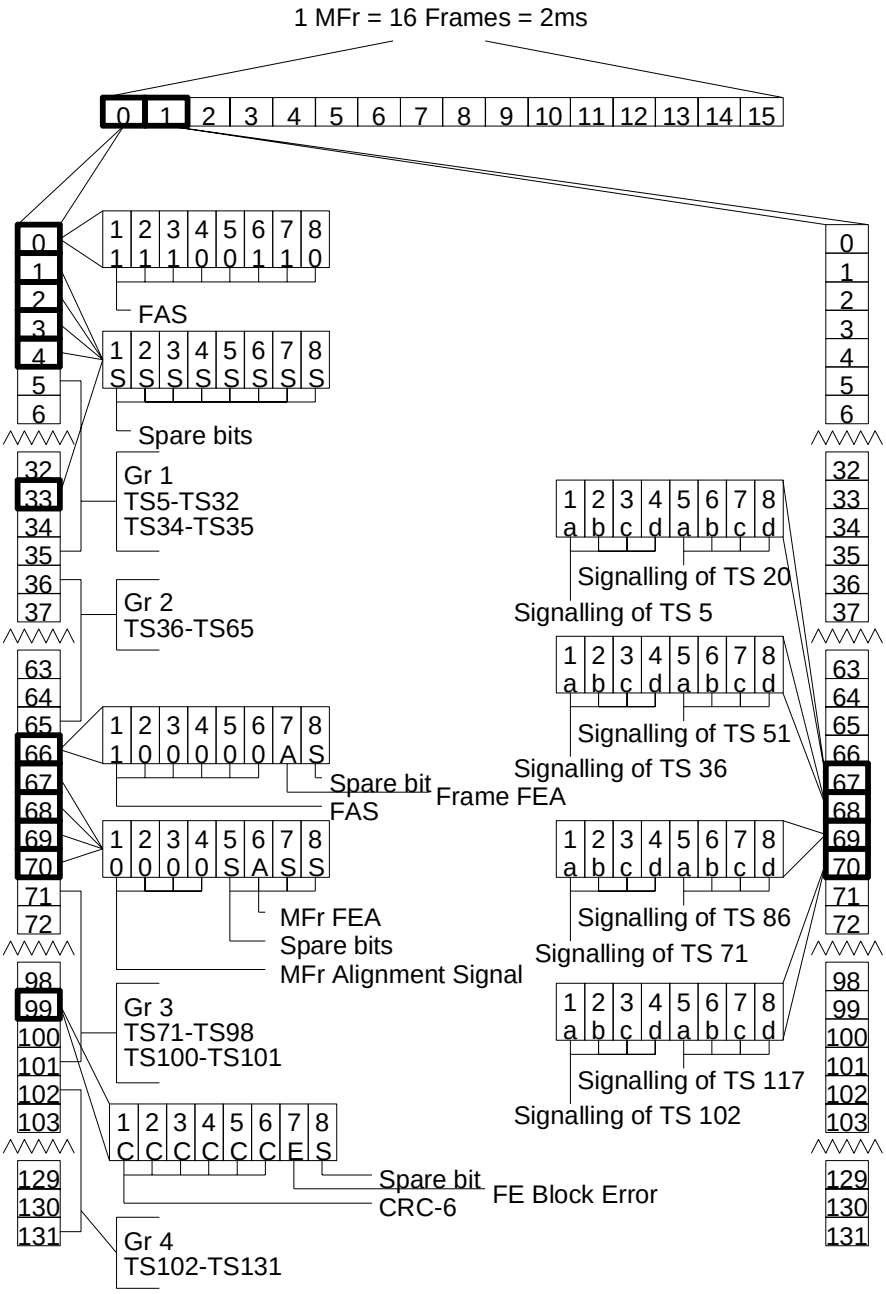
Multiframe Buffers			
Frame buffer mode	Multiframe buffer mode	MFr-Rx delay	MFr-Tx delay
2 frames	2 MFr	0…2 MFr	0 Fr
4…8 frames	2 MFr	0…2 MFr	1 Fr
64 frames	4 MFr	1…3 MFr	1 Fr

The length of a frame is 125 μs; the multiframe length is 2 ms.

In both multiframe buffer modes the centring is triggered if the distance between the received multiframe phase and the X-bus multiframe phase is less than one frame. In a buffer with two multiframes the centring is made by moving the write address one multiframe further, which means that the information of one multiframe is lost or repeated. In a buffer with four multiframes the centring means that the information of two multiframes is lost or repeated.

In GMH and cross-connect units the time slot data and signalling data have separate buffers. Therefore there are different delays in the processing of signalling data and time slot data. This means that the signalling data and time slot data which are placed in a transmitted frame do not necessarily originate from the same frame.

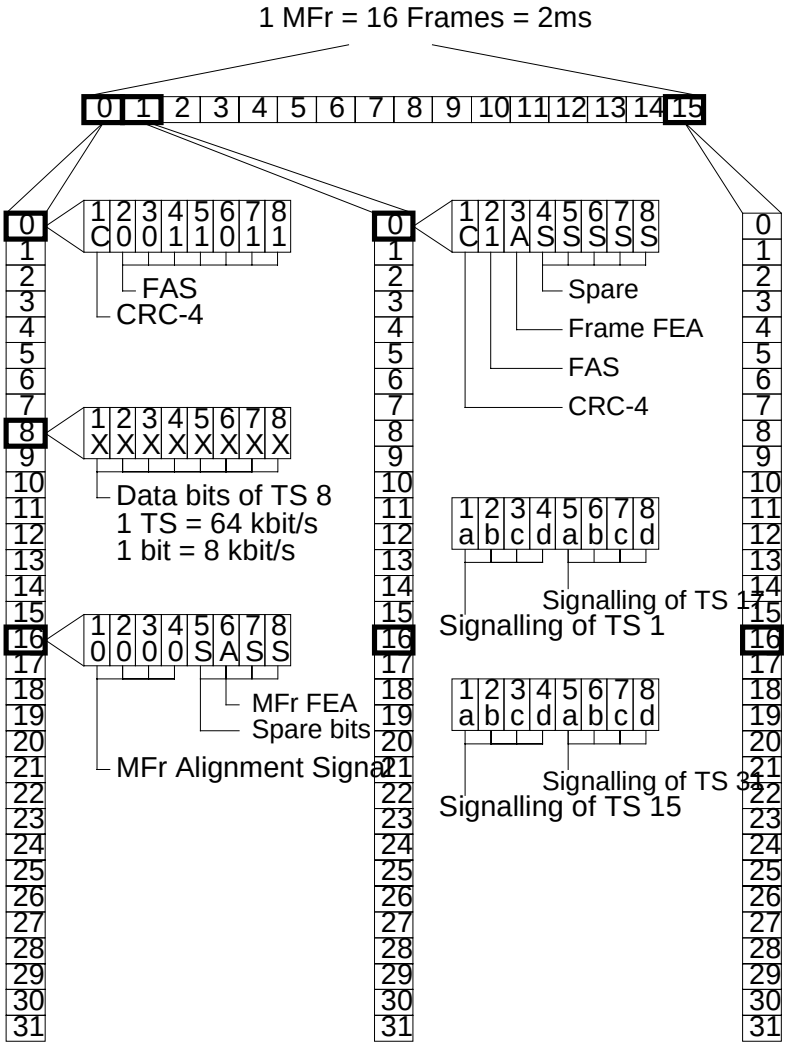
8448 kbit/s Frame Structure



1 Frame = 132 TS = 1056 bits = 125 µs

G.704 8448 kbit/s

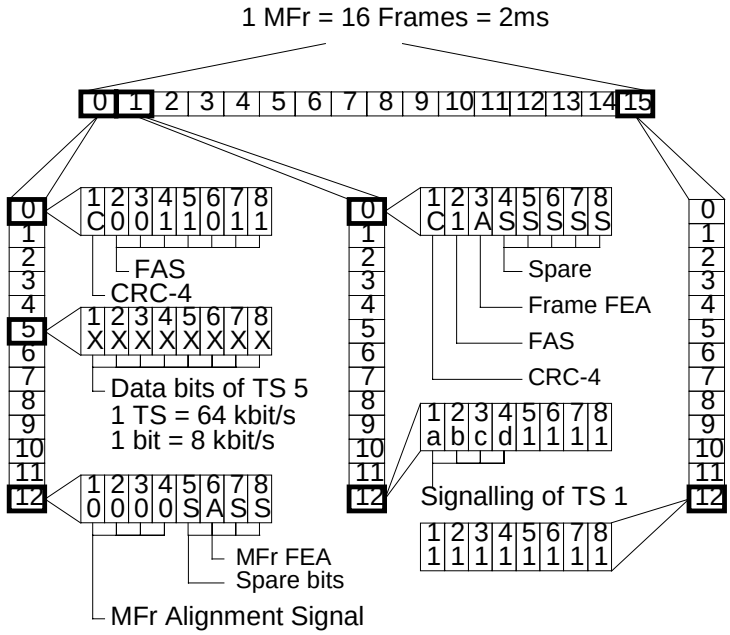
2048 kbit/s Frame Structure



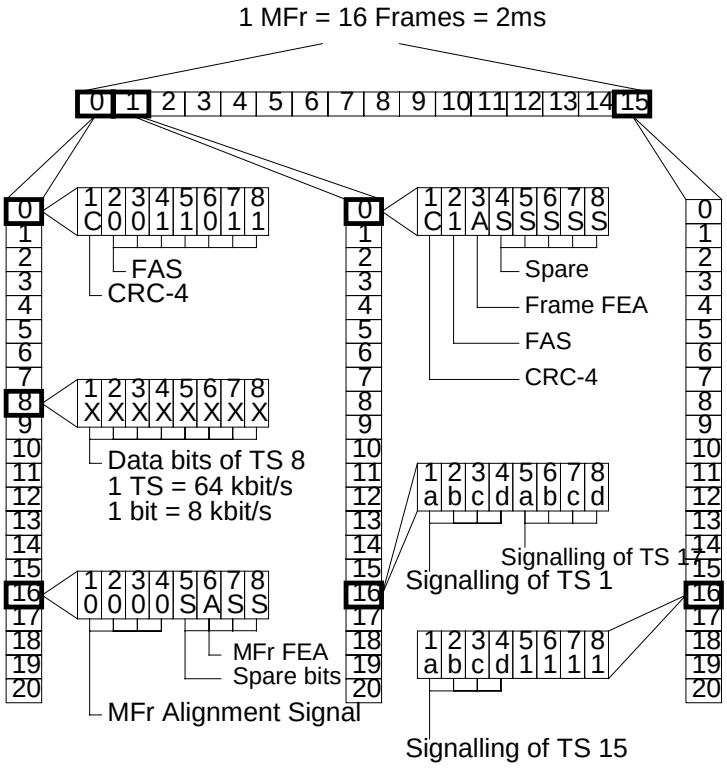
1 Frame = 32 TS = 256 bits = 125 µs

G.704 2048 kbit/s

N x 64 kbit/s Frame Structure



1 Frame = 13 TS = 104 bits = 125 µs



1 Frame = 20 TS = 160 bits = 125 µs

Multiframe Structure in the Signalling Time Slot

(8 Mbit/s frame ts67, 68, 69, 70. 2 Mbit/s frame and n x 64 kbit/s frame with n >17 ts16. N x 64 kbit/s frame with n≤17 tsn-1.)

Frame #	**Sigtsbits 1234 abcd**	**Sigtsbits 5678 abcd**	**Use**
0	0000	SASS	0000=M-FSW, A=FEA (1-active), S=spare
1	ts1	ts17	abcd bits for ts1 and ts17 of the group
2	ts2	ts18	
3	ts3	ts19	
4	ts4	ts20	
5	ts5	ts21	
6	ts6	ts22	
7	ts7	ts23	
8	ts8	ts24	
9	ts9	ts25	
10	ts10	ts26	
11	ts11	ts27	
12	ts12	ts28	
13	ts13	ts29	
14	ts14	ts30	
15	ts15	ts31	abcd bits for ts15 and ts31 of the group

Multiframe length is 16 frames/125 μs = 2 ms (500 Hz)

CRC Multiframe Structure in ts0 for the 2 Mbit/s and n x 64 kbit/s Frames

Frame #	**ts0 bits**		**Use**
	1	**2345678**	
Block #1			
0	C1	0011011	C1…C4 = CRC-4 bits
1	**0**	1ASHHHH	A = FEA (1-active), S = spare
2	C2	0011011	0011011 = FSW, H = reserved for the HDLC link
3	**0**	1ASHHHH	**001011** = CRC M-FSW
4	C3	0011011	
5	**1**	1ASHHHH	
6	C4	0011011	
7	**0**	1ASHHHH	
Block #2			
8	C1	0011011	
9	**1**	1ASHHHH	
10	C2	0011011	
11	**1**	1ASHHHH	
12	C3	0011011	
13	E1	1ASHHHH	E1 = BlockI FEA (0-active)
14	C4	0011011	
15	E2	1ASHHHH	E2 = BlockII FEA (0-active)

The CRC multiframe length is 16 frames/125 μs = 2 ms (500Hz).

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